A WIDEBAND QUADRATURE VCO USING A NOVEL TAIL CURRENT-CLIPPING TECHNIQUE

A Thesis

by

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MASTER OF SCIENCE

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ABSTRACT

This thesis presents a Quadrature VCO (QVCO) architecture using a novel tail current-clipping technique that improves the phase noise performance of a traditional QVCO by about 4 dB while obtaining a tuning range of about 4 to 5 GHz. This work introduces an innovative idea based on a new approach of implementing a QVCO without an explicit conventional parallel or series coupling network and eliminates some of the issues associated with a traditional QVCO such as bimodal oscillations and phase noise degradation due to the coupling network.

The proposed structure has a lot of advantages over the traditional P-QVCO in terms of both phase noise and power consumption. The proposed QVCO was fabricated in the 40 nm CMOS technology. The measured phase noise at 4.9 GHz was about -123.2 dBc/Hz at 1 MHz offset frequency while the quadrature error was less than 3° over the complete tuning range. The proposed architecture consumes a power of about 7.5 mW from a supply of 1.1 V with a figure-of-merit (FoM) of 188.27 dBc/Hz at 4.9 GHz output frequency.

DEDICATION

To my Amma and Appa.

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All work conducted for the thesis was completed by the student independently.

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TABLE OF CONTENTS

Page

LIST OF FIGURES

FIGURE Page

LIST OF TABLES

TABLE Page

1. INTRODUCTION

1.1 Prevalence of Quadrature VCOs

Quadrature VCOs are indispensable to state-of-the-art RFICs and High-Speed Wireline Links. It's interesting to note that the need for accurate quadrature signals was there even during 1950s in systems like Costas Loop, Digital Modulation schemes like QPSK, QAM etc. The uses of quadrature signals are enormous. New state-of-the-art tranceivers rely heavily on accurate quadrature signals, and this trend will continue even in the future. The fact that both cosine and sine are orthogonal signals has resulted in so many advantages.

1.1.1 Wireless Communication

Most of the popular digital communication techniques make use of inphase and quadrature signals for modulation. This includes techniques like QPSK, QAM etc. Recently, such techniques have also found their uses in Optical Communication ICs. A simple transmitter (TX) architecture is shown in Figure 1.1. They are commonly used in quadrature down

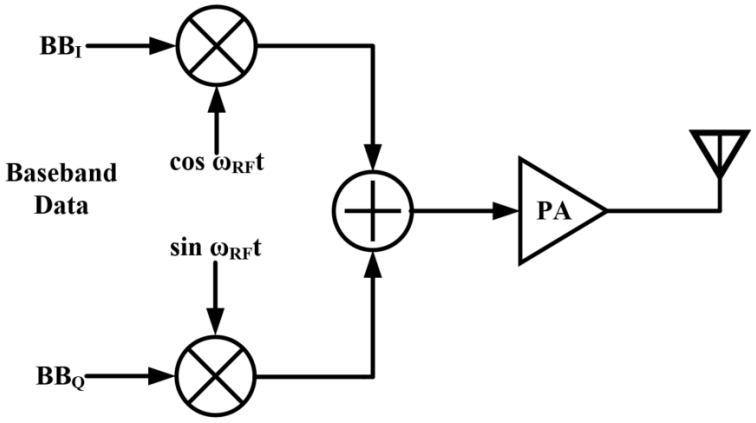

Figure 1.1: A traditional I/Q TX that requires quadrature signals for upconversion.

conversion, zero-IF receivers, image-reject receivers etc. In zero-IF receivers, quadrature downconversion is required to avoid self-corruption due to asymmetric spectrum of RF data [8]. This is shown in Figure 1.2 with the spectrum at each point along the receiver chain. The I/Q baseband data distinguishes the positive and negative frequency components, which helps in avoiding self-corruption. I/Q receivers are also referred to as complex receivers. In all these systems, the effect of quadrature mismatch has a pro-

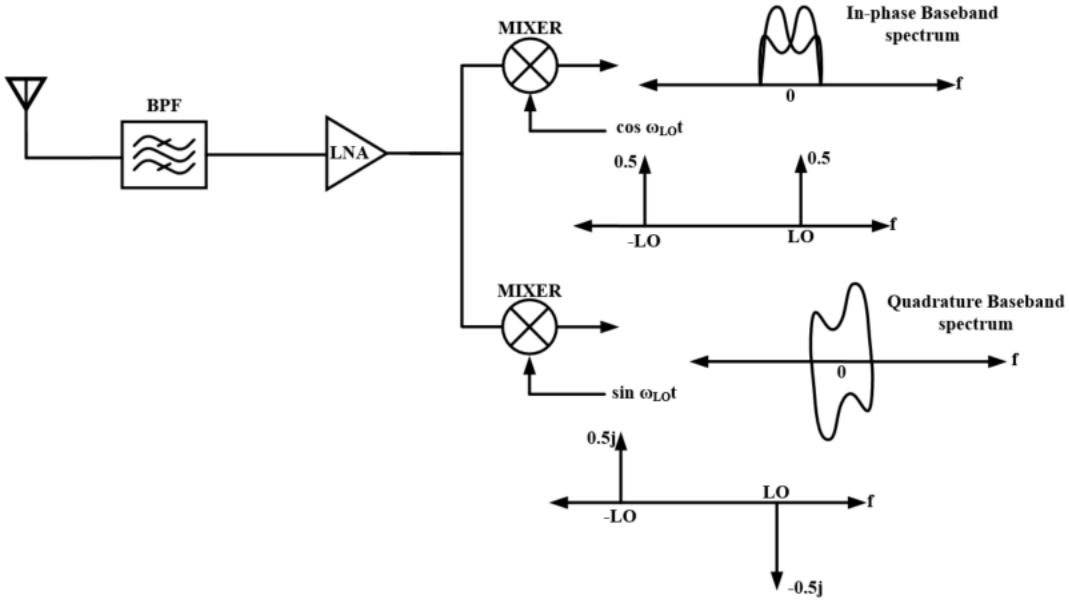

Figure 1.2: Zero-IF RX requires quadrature downconversion to separate I and Q in order to avoid self-corruption. The spectrum of the signal along the RX chain is shown as well.

found impact on the performance of the tranceiver. For example, I/Q mismatch would result in distortion in the constellation and degrades the Error Vector Magnitude (EVM) and hence Bit Error Rate (BER) of the entire system. I/Q mismatch can also cause poor image rejection in zero-IF and image-reject receivers. Cognitive Radios (CRs) make use of single-side band (SSB) mixers for increasing the frequency range. SSB mixers require

quadrature signals for obtaining a single-side band. One thing to note here is that, like in any other VCOs, the phase noise of QVCO is equally critical to mitigate reciprocal mixing. Therefore, there is a huge demand for accurate and low phase noise Quadrature VCOs in wireless communication systems.

1.1.2 Wireline Communication

Wireline Communication didn't see the uses of QVCOs until recently in half-rate architectures. High-Speed IO links such as PCIe, USB etc., have seen a steady increase in the data rate. This comes at the expense of reduction in power efficiency. By using quadrature signals, High-Speed Clock and Data Recovery (CDR) loops employ half-rate architecture to avoid generating clock signal at the data rate, but at half the data rate. As the maximum frequency of operation is half of what it would be otherwise, the power efficiency improves drastically amd this also helps in improving the timing margin. Almost most of the very high-speed IO link receivers use half-rate architectures especially when the data rate is above 10 Gbps. One of the key features of quadrature signals, as explained before, is the means of generating multiple phases of a clock signal with respect to a reference clock by weighted combination of the quadrature signals. Phase Interpolators (PIs) use this property to lock the phase of the clock with that of the data. Unlike Wireless Communication, the absolute value of phase noise at a frequency offset is not of great importance. Instead, the main Figure of Merit (FOM) is the root mean square value of the jitter (rms jitter). Jitter is related to the phase noise spectrum through integration. An increase in the total power of a phase noise spectrum would result in an increase in the jitter. This degrades the BER and hinders the possibility of increasing the data rate of the link. Any phase mismatch between quadrature signals would result in a deterministic jitter and would cause an overhead in the timing margin. Hence it's important to have low jitter, accurate QVCOs even in wireline communication systems.

1.2 Motivation

Quadrature VCOs have seen widespread usage in many applications described before. One of the key challenges is in reducing the phase noise and phase mismatch at the same time. Cognitive Radio applications need wide frequency tuning range while at the same time require very low phase noise and phase mismatch. It's well known that there is a trade-off between tuning range and phase noise [**?**]. In addition, there is also a trade-off between phase noise and phase mismatch [9]. For all these reasons, designing a QVCO that meets all the specifications is generally challenging. Quadrature signals can be obtained by RC filters, ring oscillators, delay-locked loops, frequency dividers, coupling two LC oscillators (QVCO) etc. The architecture that has been prevalent in the literature is the one based on coupling two LC oscillators to generate quadrature signals, which will be referred as QVCO (or Parallel-QVCO) for the sake of simplicity. The first QVCO was introduced in ISSCC 1996 [10]. During the last decade, there has been a tremondous amount of research work on improving the Parallel-QVCO (P-QVCO) architecture Despite the improvments to the architecture, most of the designs tend to use frequency dividers for generating quadrature signals because of the degradation in the phase noise performance of the QVCO due to the coupling network and other issues associated with it. The main motivation behind this thesis is to revisit the traditional architectures that are present in the current literature and introduce an idea that could potentially mitigate the effects of the trade-offs mentioned before.

1.3 Research Contribution

This research work introduces a method to improve the phase noise performance of a QVCO by shaping the tail current source and an innovative architecture for the QVCO coupling network. Similar to superharmonic coupling, the issue of bimodal oscillations is eliminated without adding additional noise due to the coupling network. The design

is superior to the traditional superharmonic coupling techniques reported in the literature. Using this idea, an improvement in the phase noise of about 4 to 5 dB has been achieved. The design has been fabricated in 40nm CMOS technology node.

1.4 Thesis Organization

This thesis is organized as follows. Chapter 2 discusses the basics of QVCO architecture and surveys the existing and latest architectures in the literature. Chapter 3 introduces the proposed QVCO. Chapter 4 discusses in detail about simulation and measurement results. The thesis is concluded with the final chapter that draws the summary of this research work along with the potential improvements for future work.

2.1 Basics of QVCO

The first QVCO was presented in ISSCC 1996 [10]. The underlying idea is shown in Figure 2.1. This can be represented using a simplified model, as shown in Figure 2.2.

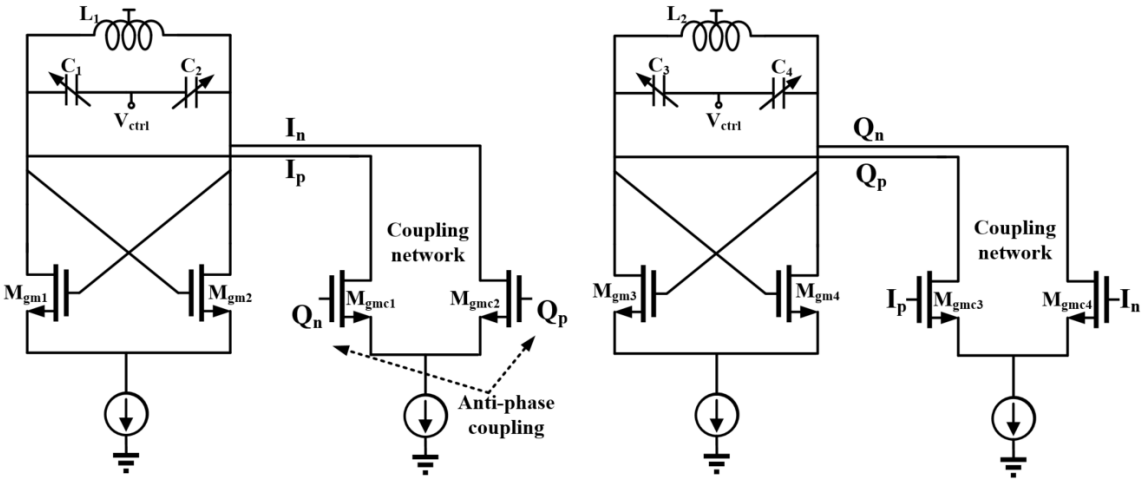

Figure 2.1: A traditional QVCO architecture [1]

Based on Figure 2.2, the following equations are obtained.

$$V_1 = -(V_1 G_m + V_2 G_{mc}) Z(s)$$

$$V_2 = -(V_2 G_m - V_1 G_{mc}) Z(s)$$

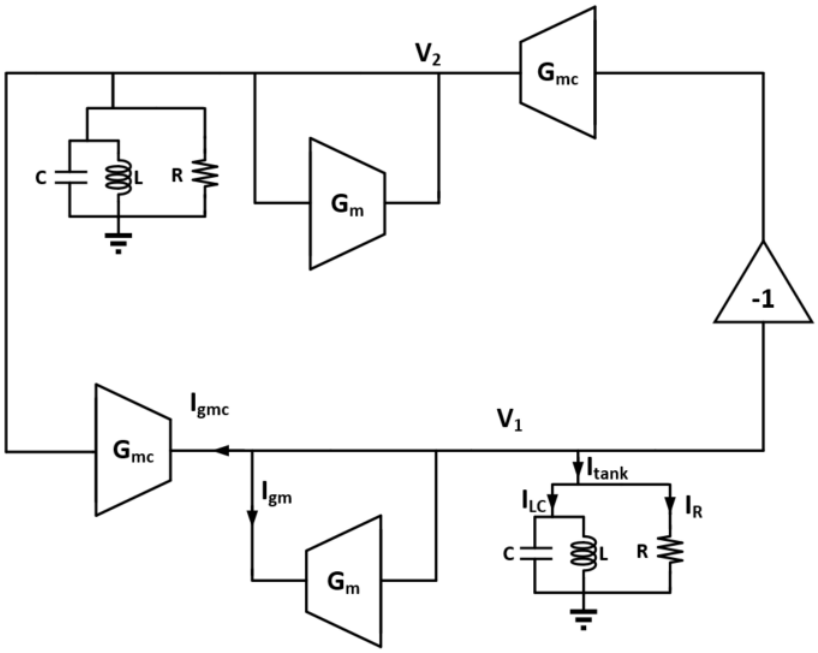

Figure 2.2: QVCO model [1]

This can be simplified as,

$$\frac{V_1}{V_2} = \frac{V_1 G_m + V_2 G_{mc}}{V_2 G_m - V_1 G_{mc}}$$

$$V_1 V_2 G_m - V_1^2 G_{mc} = V_1 V_2 G_m + V_2^2 G_{mc}$$

$$V_1 = \pm j V_2 \tag{2.1}$$

Therefore, V_1 and V_2 are 90° out of phase with respect to each other and quadrature signals are obtained. A simple way to look at this structure is shown in Figure 2.3. In order to satisfy Barkhausen criteria, two VCOs should produce 90° phase shifts with respect to

each other. A direct consequence of Eq. (2.1) is that there are two possible solutions for the above architecture. It's not certain whether V_1 lags or leads V_2. There are several issues

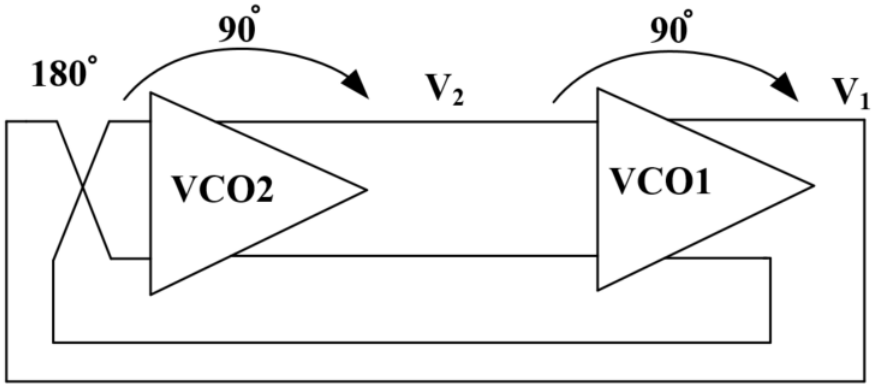

Figure 2.3: A simplified QVCO model based on Barkhausen criteria

associated with this architecture for this reason and the issues are discussed as follows.

2.1.1 Bimodal oscillations

Consider the architecture show in Figure 2.1. The currents are represented in vector diagrams, as shown in Figure 2.4. Based on Eq. (2.1), there are two possible solutions that correspond to Figures 2.4(a) and (b). Note that the vector I_R is in phase with V_1 with the magnitude determined by $\frac{V_1}{R}$.$|I_R|$ is also equal to $|I_{gm}|$ $(= G_m V_1)$. The problem lies in the fact that the tank current I_{tank} is phase shifted from I_R and hence V_1 by θ. This means the tank circuit should have V_1 and I_{tank} with a non-zero phase difference between them. For any tank circuit, this is possible only if the frequency is off from the resonant frequency, as shown in Figure 2.5. There are two possible frequencies of operation corresponding to either $+\theta$ or $-\theta$. This results in bimodal oscillations and an ambiguity exists. In addition, it has several problems associated with it. The tank circuit is no longer at the resonant

frequency. The Q factor of a tank circuit is maximum at the resonant frequency. One way to define Q factor for an LC tank circuit is given in Eq. (2.2) [8]. Here ϕ corresponds to phase of Z(s) of the tank circuit. Since the slope of ϕ is maximum at the resonant frequency, Q factor is also maximum at the resonant frequency. Hence any deviation from the resonant frequency would result in a reduction in the Q factor and hence degradation in the phase noise performance of the QVCO.

$$Q = \frac{\omega_0}{2} \left| \frac{d\phi}{d\omega} \right| \tag{2.2}$$

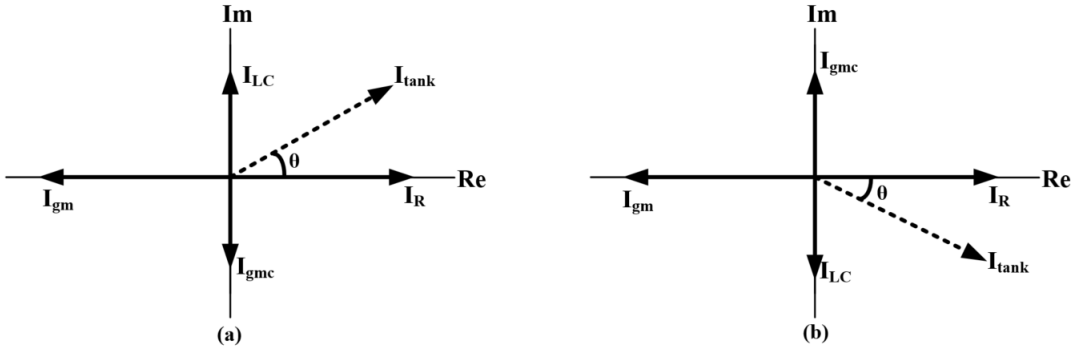

Figure 2.4: (a) Current vector plots when V_1 lags V_2 and (b) Current vector plots when V_1 leads V_2

Here the angle θ is given by,

$$\theta = tan^{-1}\left(\frac{I_{LC}}{I_R}\right) = tan^{-1}\left(\frac{I_{gmc}}{I_{gm}}\right) \tag{2.3}$$

If G_m and G_{mc} transistors have the same current density or $\frac{gm}{I_d}$, then

$$\theta = tan^{-1}\left(\frac{G_{mc}}{G_m}\right) = tan^{-1}(m) \tag{2.4}$$

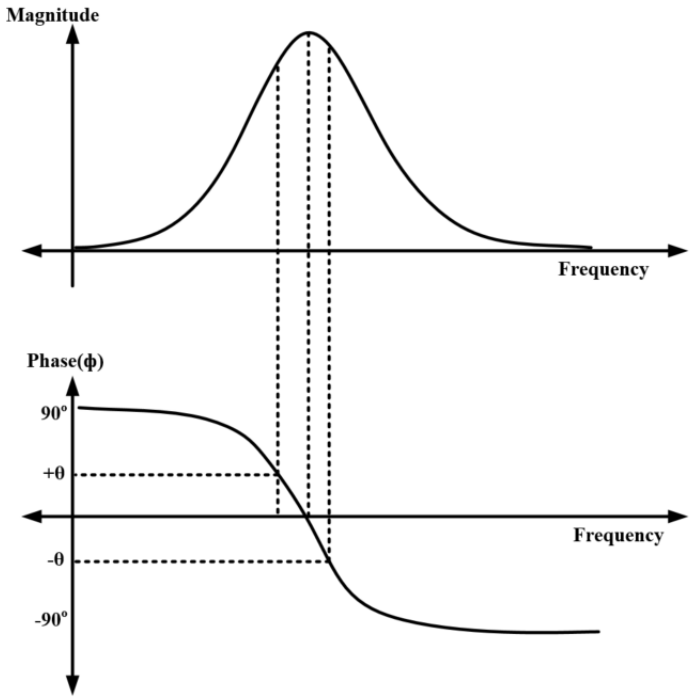

Figure 2.5: Magnitude and Phase response of the impedance for an LC tank circuit. θ corresponds to the phase shift between V_1 and I_{tank} needed for the QVCO.

Here, m is the coupling factor defined by $m = \frac{G_{mc}}{G_m}$. As the coupling factor m increases, the phase deviation also increases and hence the frequency deviation increases. This is bad in terms of phase noise performance. Whereas, if the coupling factor is very small, locking may not be guarenteed in the presence of mismatches between the two VCOs. As will be discussed shortly, weak coupling results in large phase error in the presence of mismatches. Hence there is a trade-off in choosing the right value for m. Typically, m is chosen to be around 0.2 to 0.25.

Though there are two solutions for the above architecture, for a typical lossy inductor, an LC resonant circuit generally has higher impedance magnitude at higher frequency mode than at the lower frequency mode for the same phase ϕ, as shown in Figure 2.5. For this reason, the mode with higher loop gain dominates and the QVCO oscillates at the

mode with higher frequency. This difference in loop gains is very small when the LC Q factor is high, which is required for good phase noise performance. Therefore, the exact mode of oscillation is very sensitive to delays along coupling path and any asymmetry. For these reasons, there is always an ambiguity.

One way to eliminate bimodal oscillations is to introduce a phase delay along the coupling path [11], as shown in Figure 2.6. Using this approach, one mode of oscillation

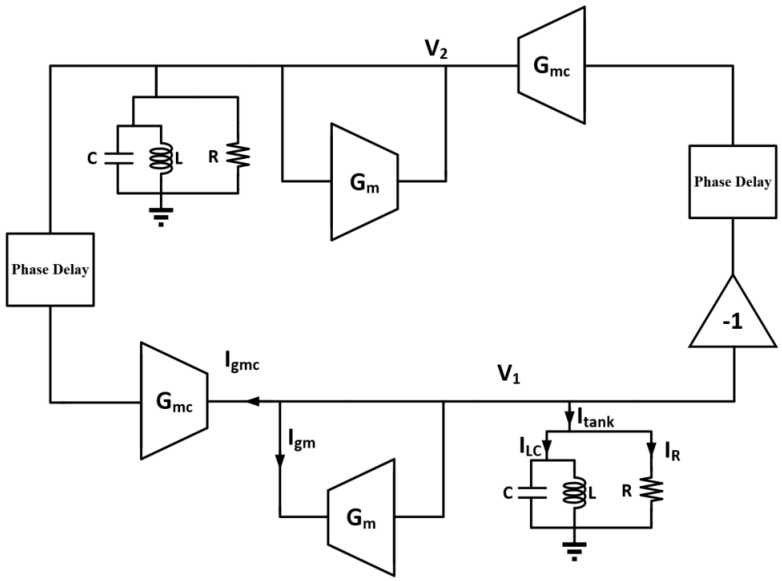

Figure 2.6: QVCO model with a phase delay along the coupling paths

can be intentionally made to have higher loop gain than the other mode, as explained as follows. In the presence of phase delay, say ψ,

$$V_1 = -(V_1 G_m + V_2 G_{mc} e^{-j\psi}) Z(s)$$

$$V_2 = -(V_2 G_m - V_1 G_{mc} e^{-j\psi}) Z(s)$$

It can be shown that, $V_1 = \pm jV_2$. Therefore, two QVCOs still operate in quadrature with respect to each other. Though there are two solutions, one mode is made to have higher loop gain than the other one. This can be explained using Figure 2.7. Since θ_1 is smaller than θ_2, mode (a) in the above figure dominates, as the loop gain is higher for mode (a) based on the tank response of the LC circuit shown in Figure 2.5.

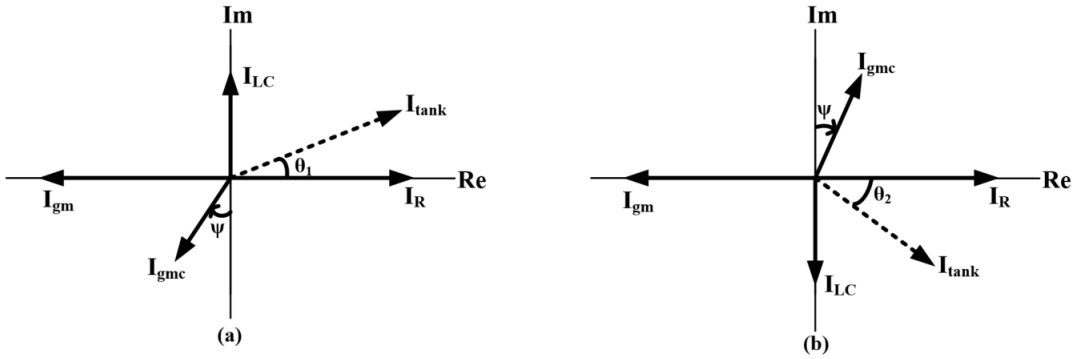

Figure 2.7: In the presence of phase delay, (a) Current vector plots when V_1 lags V_2 and (b) Current vector plots when V_1 leads V_2. Arrow on angle ψ indicates that the vectors are delayed in phase.

2.1.2 Phase noise and Phase accuracy trade-off

The architecture shown in Figure 2.1 inherently suffers from a trade-off between phase noise and phase accuracy. This has been explained extensively in [9]. It was shown previously that an increase in the coupling factor m would result in more deviation of the frequency of oscillation from the resonant frequency. Since the Q factor decreases as the frequency deviates from the resonant frequency, the phase noise performance also degrades with increase in the coupling factor m. On the other hand, a very low coupling factor m might not completely lock the two VCOs if the LC resonant frequencies of the two VCOs are mismatched. In addition, when the resonant frequencies are mismatched,

the two VCOs are no longer quadrature with respect to each other. Instead, there is a non-zero error from the ideal 90° phase difference. This is shown in Figure 2.8. Here ω_1 and

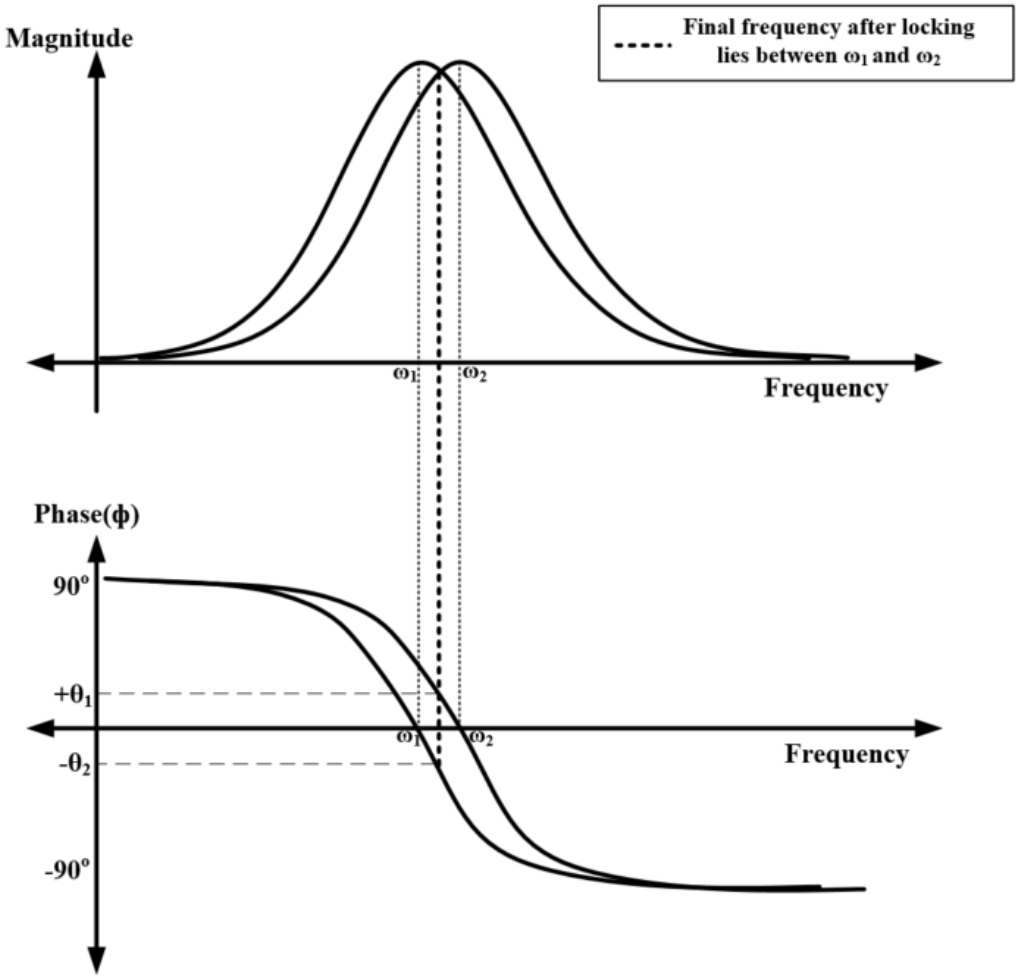

Figure 2.8: Magnitude and phase of impedance Z(s) of two LC VCOs in the QVCO when there is a mismatch in the resonant frequency.

ω_2 are the resonant frequencies of tank circuits of the two VCOs. As the resonant frequencies aren't the same, the oscillators lock at an intermediate frequency that lies between ω_1 and ω_2. Due to this reason, the LC tanks of two VCOs should now incur phase shifts θ_1

and $-\theta_2$, as shown in Figure 2.8. In the presence of mismatch, the tank current vector undergoes an additional phase shift $d\theta$, as shown in the Figure 2.9. In order to accomo-

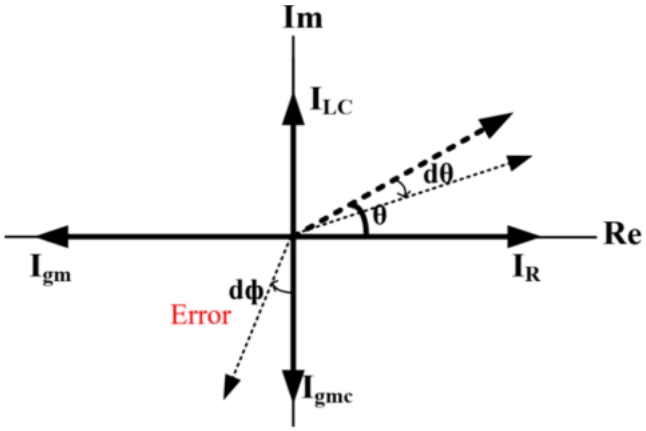

Figure 2.9: Current vectors in the presence of mismatch in the resonant frequencies of the two VCOs.

date for this additional phase shift $d\theta$ in the resultant vector, the two VCOs much incur an additional phase difference $d\phi$. If the coupling coefficient m ($= \frac{I_{gmc}}{I_{gm}}$) is large, then $d\phi$ that is required to compensate for this additional phase shift in the tank current vector will be small. Intuitively, if I_{gmc} is larger than I_{gm}, the vector I_{gmc} just has to rotate a little to compensate for the phase shift $d\theta$, as obvious from the Figure 2.9. It can be shown that [9] the phase error $d\phi$ is given by:

$$d\phi = \frac{\left(1 + \frac{1}{m^2}\right) d\theta}{2} \approx \frac{Q}{m^2} \frac{d\omega}{\omega_{osc}} \tag{2.5}$$

In Eq. 2.5, $d\omega$ corresponds to the mismatch in the resonant frequencies of the two VCOs from the frequency of locking. Hence a high coupling ratio m results in better phase accuracy of the QVCO. High Q factor also results in a huge phase error. This make sense intutively, as high Q factor corresponds to a steep change in the phase of the impedance

characteristics about the resonant frequency and the additional phase change would be very sensitive to the mismatch in the resonant frequencies. To improve phase accuracy, high coupling factor is required, and to reduce phase noise, low coupling factor is required. Therefore, there is inherently a trade-off between phase noise and phaser accuracy. Another issue is that the coupling network contributes noise and degardes the phase noise performance.

2.2 Other QVCO architectures

In this section, some of the other QVCO architectures that have been reported in the literature are discussed.

2.2.1 Series QVCO

The architecture described in Figure 2.1 is sometimes referred to as Parallel QVCO (P-QVCO), as the coupling transistors are in parallel with the main cross coupled pair. It's possible to couple two VCOs through series coupling transistors, explained in [2]. This is known as Series QVCO (S-QVCO) and has some advantages over P-QVCO. The basic diagram is shown in Figure 2.10. A model similar to the one shown in Figure 2.2 holds true in the case of S-QVCO [2]. It can be shown that for the same coupling factor, S-QVCO offers better phase noise performance than P-QVCO. The reason is because M_{gmc1} and M_{gmc2} noise sources are degenerated by M_{gm1} and M_{gm2} as they appear at the output. Also, M_{gm1} and M_{gm2} add less noise because they are mostly in triode. It can be shown that the flicker noise due to M_{gmc1} and M_{gmc2} modulates the output frequency less than it does in the case of P-QVCO [2]. This architecture still suffers from bimodal oscillations similar to P-QVCO. The main drawback of this architecture is that there are cascode transistors and the supply needs to be high enough to ensure that the bias conditions for all the transistors aren't affected. This makes it less attractive for advanced technology nodes, where the supply is low, and this trend is expected to continue in the future.

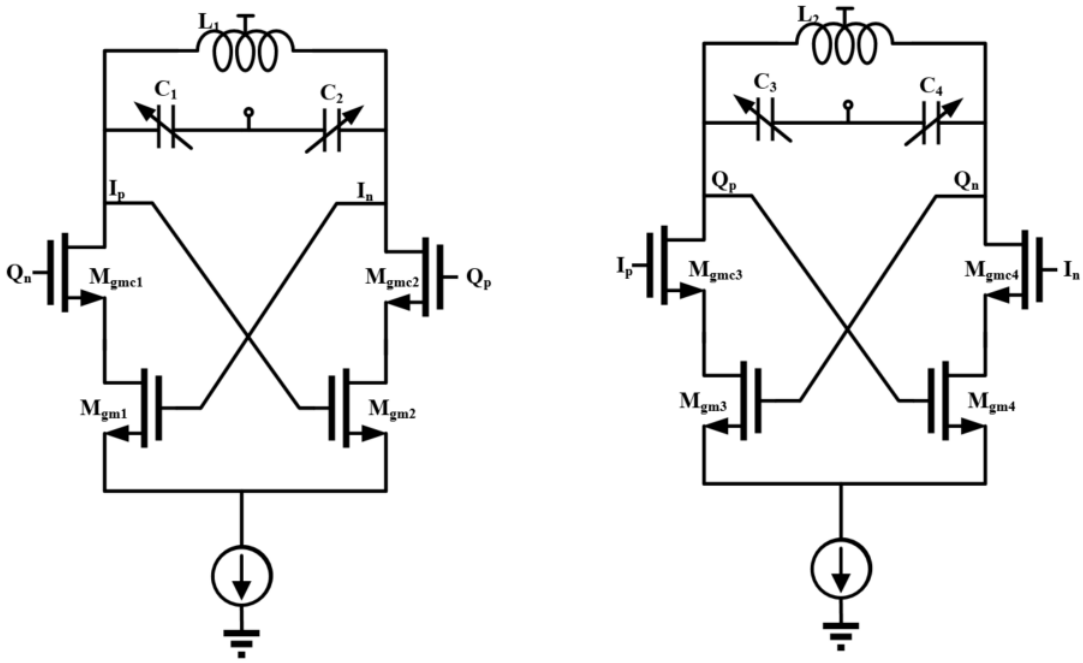

Figure 2.10: Series QVCO [2]

2.2.2 QVCOs using Superharmonic Coupling

The main problem with P-QVCO and S-QVCO architectures is that the bimodal oscillations severely degrade the phase noise performance and cause ambiguity in the output frequency. Another idea, which was introduced in [3], to get quadrature signals is to couple two VCOs through superharmonic coupling. This is achieved by coupling $2f_{osc}$ signals at the tail nodes, where f_{osc} is the frequency of oscillation. The architecture that was proposed in [3] is shown in Figure 2.11. The idea behind this architecture is as follows. The tail nodes V_A and V_B oscillate at $2f_{osc}$. If I and Q outputs are to be quadrature signals, then V_A and V_B should be anti-phase with respect to each other. Using a transformer structure with the direction of coupling shown in Figure 2.11, it's possible to make a QVCO. The coupling currents through the inductors L_5 and L_6 are at $2f_{osc}$. These signals get down-converted by the cross-coupled transistors $M_{gm1} - M_{gm4}$ to f_{osc}. The two VCOs therefore

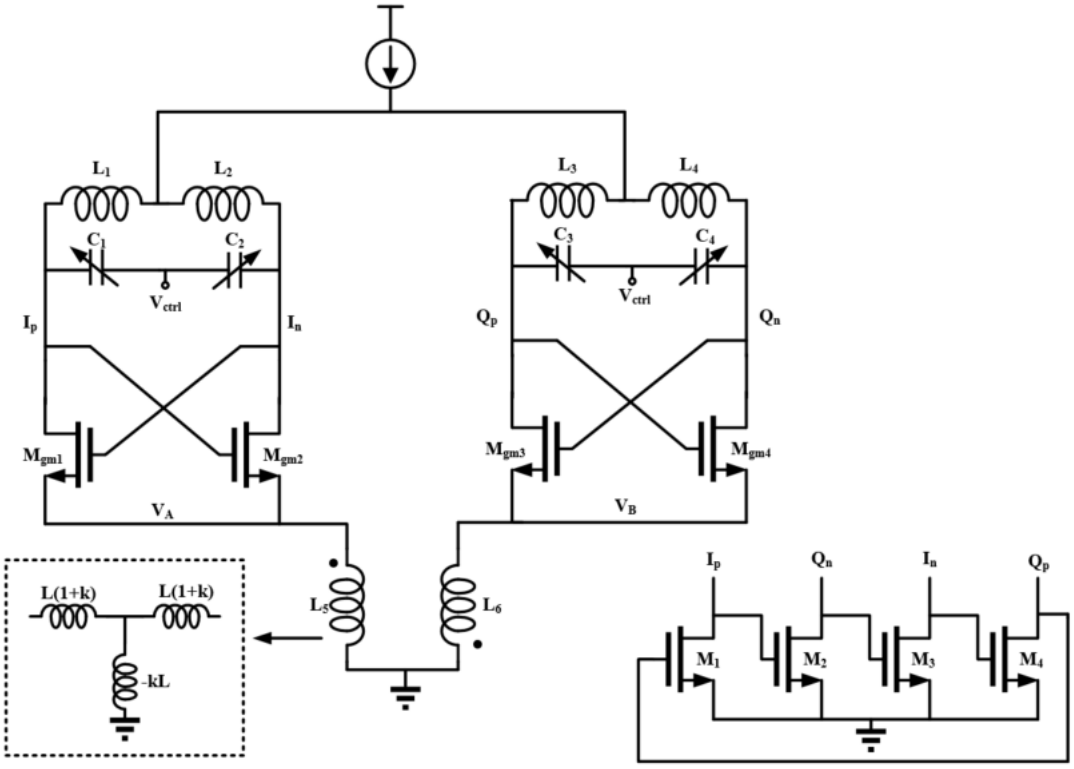

Figure 2.11: Superharmonic coupled QVCO using transformers [3]

operate in quadrature with respect to each other to satisfy this condition. There is another solution that corresponds to zero phase difference between the two VCOs. The former is called the odd-mode, and the latter is called the even-mode of oscillation. During even-mode, both V_A and V_B are in-phase with respect to each other. If $L_5 = L_6 = L$ and coupling coefficient $k = \frac{M}{\sqrt{L_5 L_6}}$, where M is the mutual inductance, then the equivalent circuit for the transformer is shown in Figure 2.11. A quick inspection of this circuit shows that the impedance or inductance seen by odd-mode component is different from that of the even-mode component at tail current nodes V_A and V_B. If L_5 and L_6 are chosen such that the equivalent inductance during odd-mode resonate at $2f_{osc}$ with the parasitic capacitances at the nodes V_A and V_B respectively, then the amplitude of oscillation increases

because this extends the current-mode regime [3]. While during even-mode, the effective inductance is small and doesn't resonate with the parasitic capacitances and hence provides lower impedance. The amplitude of oscillation during even-mode is lower than the odd-mode. Hence the QVCO loop chooses the one that has maximum magnitude of oscillation and odd-mode prevails. In this way, a quadrature VCO is obtained. The advantage of this circuit is that there is no phenonmenon of bimodal oscillation. This improves the phase noise performance. There is still an abiguity on whether I lags or leads Q. This is resolved by using weak set of transistors M_1 to M_4. Coupling between two VCOs is made through transformers which are ideally noiseless elements. There are several issues associated with this idea. First, transformers are bulky and occupy too much area on a chip. When wide range of oscillation frequency is required, L_5 and L_6 might need to be tuned so that they resonante with the parasitic capacitances at odd-mode and having tunable inductors is not a trivial task. The voltages at the nodes V_A and V_B aren't exactly sinusoidal and have components other than the second harmonic of f_{osc}, especially as the amplitude of oscillation reaches the voltage-limited regime. This needs to be taken into consideration. Regardless of these issues, this architecture shows a new way of coupling two VCOs to obtain quadrature phases without bimodal oscillations.

As transformers are bulky elements, the possibility of using capacitive coupling between the tail current nodes was explored in [4]. The architecture is shown in Figure 2.12. Similar to the previous architecture, it can be shown that [4] there are even and odd modes of oscillations. It turns out the even-mode of oscillations [4] is a metastable point and the VCOs always operate in quadrature. The coupling coefficient is determined by [4],

$$k = \frac{2C_s\omega_0 A_s}{I_{bias}}$$

In this equation, A_s is the amplitude of the sinusoidal signal at V_A and V_B. If the crosscou-

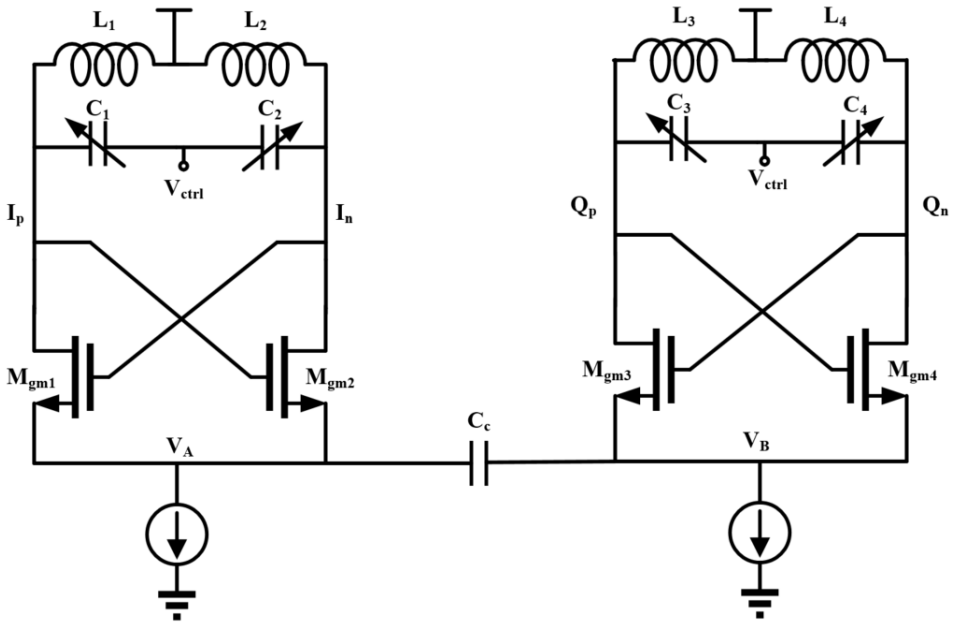

Figure 2.12: Superharmonic coupled QVCO using capacitive coupling [4]

pled transistors are sized in such a way that there is a $90°$ phase shift from the output nodes I and Q to the tail current nodes V_A and V_B, it's possible to have a tail current shaping that helps in improving the phase noise performance. The main disadvantage of this circuit is that it assumes current-limited regime of operation and that V_A and V_B have second harmonic components only. Generally, that's not the case and care needs to be taken to avoid any issue that might arise because of that. Also, tail current shaping is valid only if the active devices M_{gm1} to M_{gm4} provide the $90°$, which could be very sensitive to a lot of factors and can't be ascertained always, especially when the tuning range is large.

2.3 Noise sources in QVCOs

An important figure of merit for a QVCO is phase noise at a given offset frequency. Analyzis of noise contributors in a QVCO is less straight forward. There has been a tremondous amount of research on the phase noise analysis of VCOs and QVCOs [12],

[13], [14]. In this thesis, some of the major noise contributors to the QVCO phase noise are discussed briefly. Consider this circuit shown in Figure 2.13. In this circuit, there are

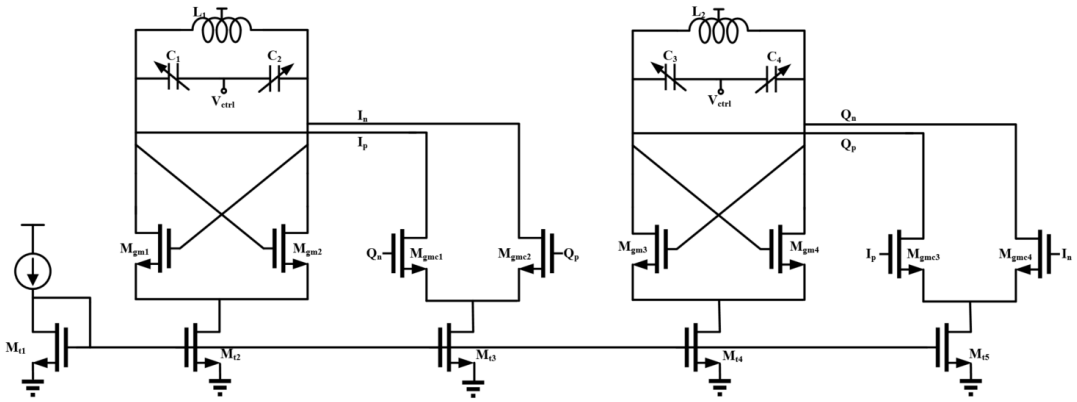

Figure 2.13: P-QVCO architecture

possibly four major sources of noise:

(i) The noise due to the losses in the resonant circuit. This can be modeled as a thermal noise in parallel with the LC tank circuit. This noise contribution can be reduced by improving the Q factor of the LC tank circuit.

(ii) The noise due to the cross-coupled transistors M_{gm1} to M_{gm4}. The noise due to switching transistors is considered in detail in [12] and [14]. The noise can be considered to be sampled by an impulse train with a period of $\frac{1}{2\omega_{osc}}$. Both device and channel noise affect the output phase noise. The upconversion of flicker noise by the switching transistors M_{gm1} to M_{gm4} is considered in detail in [13].

(iii) The noise due to tail current sources M_{t1} to M_{t5}. The channel noise at $2\omega_{osc}$ due to M_{t2}, say, gets upconverted to ω_{osc} and this appears as a Phase Modulated (PM) noise and directly affects the phase noise [8]. There have been some techniques used in the past to reduce this noise contribution by placing a capacitor in parallel to short this noise at

$2\omega_{osc}$ to ground [5], as shown in Figure 2.14. The capacitor C_T shorts the noise at $2\omega_{osc}$ at

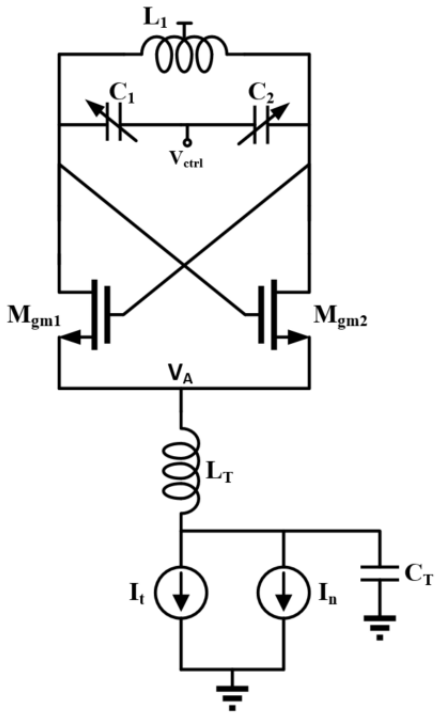

Figure 2.14: Reducing the contribution of tail current noise at $2\omega_{osc}$ using a resonant circuit [5]

the same time resonanting with L_T so that the impedance seen looking into the tail current node V_A is still huge. The flicker noise due to the tail current source gets upconverted to ω_{osc}, but it appears as an Amplitude Modulated noise (AM) rather than a PM noise [8]. Intuitively, flicker noise can be considered as a DC change in the current, and any DC change in the tail current will only affect the amplitude of the ouput signal. The problem lies in the fact that the varactors C_1 and C_2 are non-linear elements. They convert the AM noise to PM noise through AM-PM conversion [8]. This is a major contribution to the output phase noise spectrum especially at low frequency offsets such as 1 MHz, which is

crucial for RF wireless communication systems.

(iv) Another major source of noise is the noise due to coupling transistors M_{gmc1} to M_{gmc4}. Note that additional tail current sources M_{t3} and M_{t5} required to bias coupling transistors also affect the phase noise through flicker noise upconversion. For these reasons, generally QVCOs have inferior phase noise performance compared to a single VCO. The noise contribution due to M_{gmc1} to M_{gmc4} isn't as bad as M_{gm1} tp M_{gm4} as long as the coupling coefficient is small. As the coupling coefficient increases, the noise due to these coupling transistors start to dominate [12].

The tail current transistors M_{t1} to M_{t5} contribute a lot to the phase noise of the LC VCO and reducing this contribution proves to be critical for improving the phase noise performance. For this reason, recent architectures on low phase noise VCOs do not employ the tail current source [15]. Instead, variable resistors are added to eliminate the flicker noise contribution due to tail current source, as shown in Figure 2.15. Resistors don't suffer from flicker noise, and this structure completely eliminates the flicker noise contribution due to tail current source, which improves the phase noise by a huge amount. The disadvantage of this circuit is the fact that the bias current varies a lot across PVT and hence the swing changes with PVT. This can also have a poor supply rejection ratio. To solve this, an amplitude sensing network with negative feedback that controls the resistor, shown in Figure 2.16, is required, which comes at the cost of increase in power and area. The amplitude sensing network also adds its own flicker noise to the total phase noise. In addition, if the resistor value is not large enough, the Q-factor of the resonant circuit degrades for large output swings.

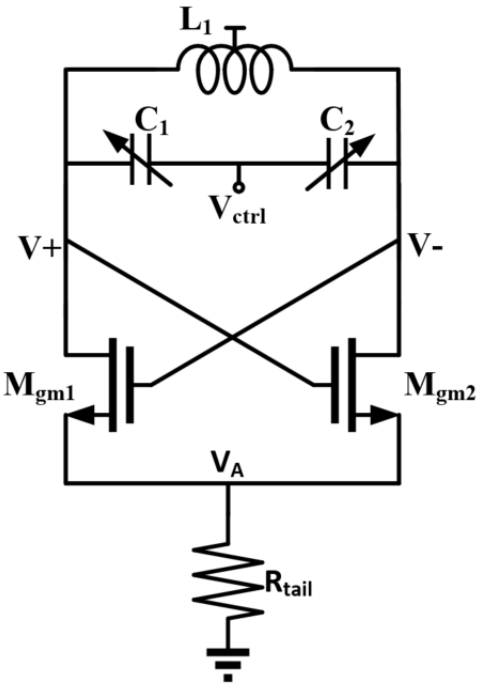

Figure 2.15: An LC VCO biased using a tail resistor

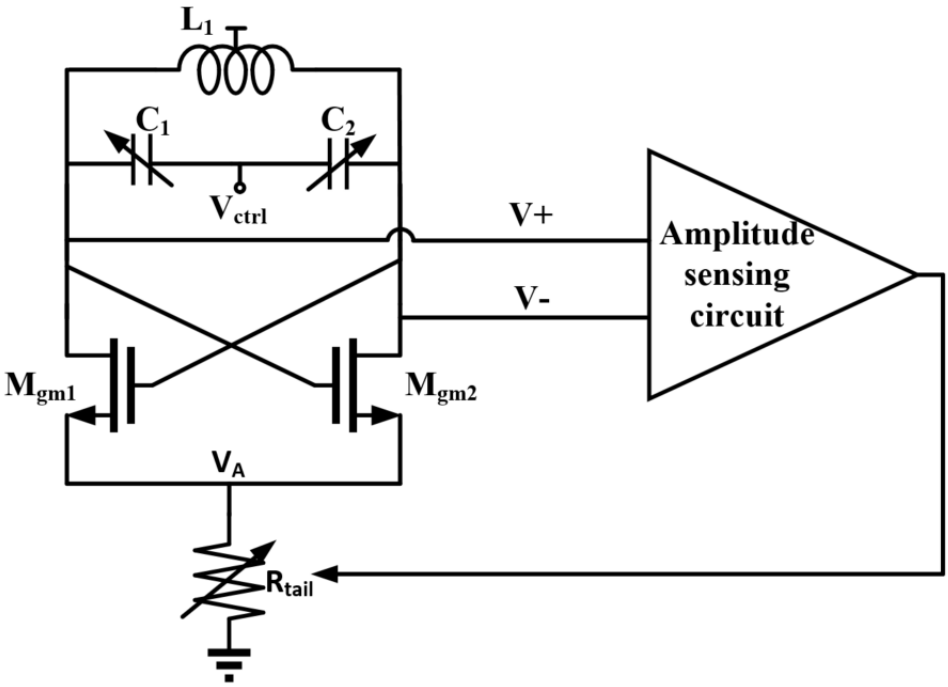

Figure 2.16: An LC VCO using an amplitude sensing and correction network [6]

2.4 Hajimiri-Lee model

2.4.1 Consequences of LTV analysis

As per the Linear Time Variant (LTV) analysis of a VCO [7], the phase change is less sensitive to the injected current (or noise) at specific time instants of the total period, which is determined by the Impulse Sensitivity Function (ISF), as shown in Figure 2.17. In this case, the current injected at instant t_2 results in more phase shift than the current injected at instant t_1. This happens because an LC oscillator is inherently an LTV system and magnitude of ISF is minimum at instant t_1 and maximum at instant t_2 . A detailed analysis of this theory is explained in the Hajimiri-Lee phase noise model [5]. Using this idea, it's

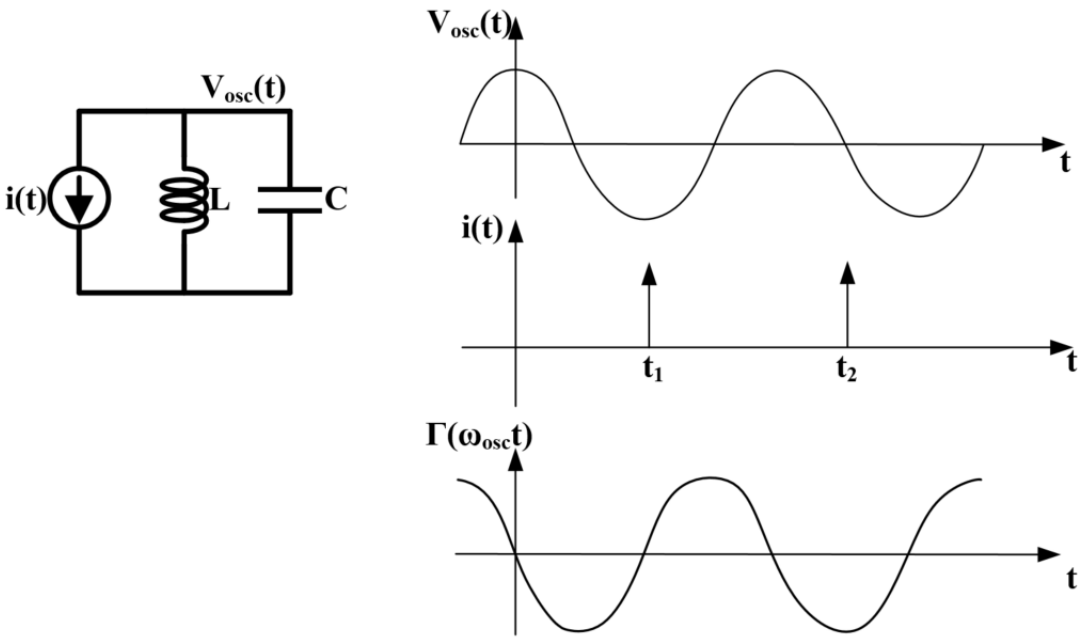

Figure 2.17: LC oscillator with input current impulses at different instants of time along with the corresponding ISF function $\Gamma(\omega_{osc}t)$ [7]

possible to modify the VCO architecture to provide the restoring energy at specific instants

of the period so that the phase noise is minimal. Note that as long as the average $|G_m R|$>1, oscillation sustains regardless of when the restoring energy is injected into the LC circuit. Here G_m is the transconductance of the restorting element and R models losses in the LC tank circuit.

2.4.2 Exploiting LTV analysis

Using the LTV analysis mentioned in the previous section, it's possible to modify the QVCO circuit and design it in such a way that the phase noise performance improves. Based on the sources of noise, it is generally observed that the flicker noise components of the tail current sources contribute a considerable amount to the total phase noise. The main sources of restoring energy include the cross-coupled transistors biased by the tail current sources. If the tail current sources are switched in such way that they are injected into the main cross-coupled transistors at those instants at which the ISF is minimum, phase noise performance could be increased. Using series switches for coupling transistors [1], the phase noise performance of the QVCO was shown to be improved. In this thesis, LTV analysis is exploited for the main tail current bias of the positive feedback network and an innovative architecture for the QVCO is proposed that improves phase noise performance by a considerable amount.

3.1 Tail current clipping

The concept of tail current clipping is introduced first. The idea is that if the tail currents in the Figure 2.13 are shaped in such a way that they are injected into the main circuit only at those instants where ISF is minimal, then the noise contribution due to tail current sources and main transistors could be reduced. This is achieved by using series switches, as shown in Figure 3.1. Assuming that I and Q are quadrature with respect to

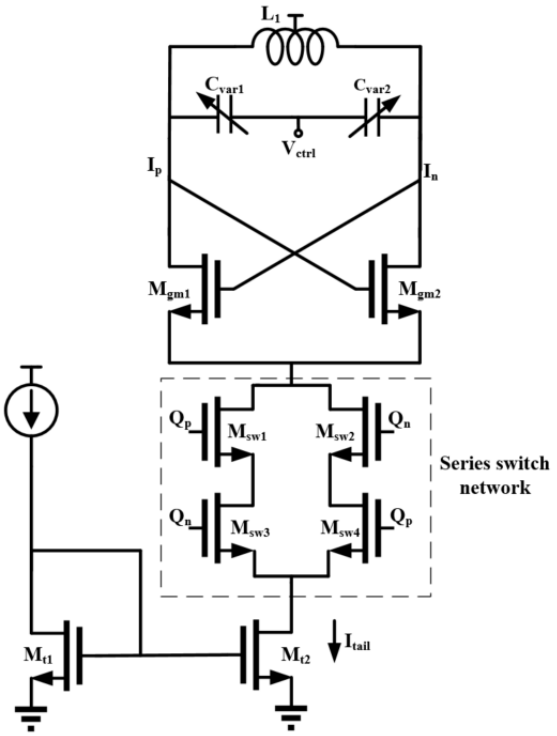

Figure 3.1: Series switches used for clipping tail current source M_{t2}

each other, the plots of output signals are shown in Figure 3.2. Consider instants t_1 and t_2.

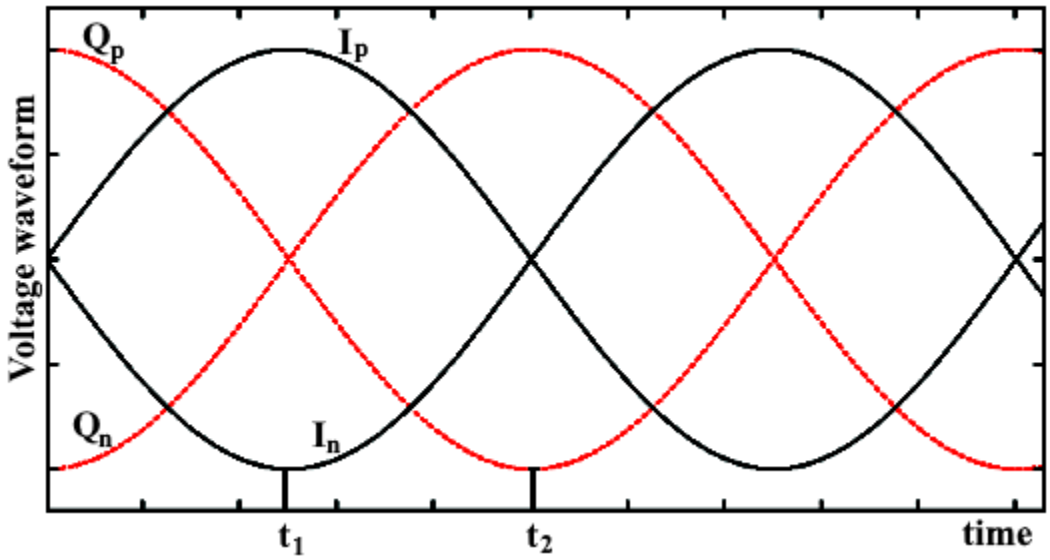

Figure 3.2: Outputs of Quadrature VCO

At instant t_1, both Q_p and Q_n are at VDD. At instant t_2, Q_p is at a low value and Q_n is at high value. If the series switches M_{sw1} and M_{sw3} are considered, the total series resistance is minimum at instant t_1 and is maximum at instant t_2. This applies to the series switches M_{sw2} and M_{sw4}. If output single swing is large enough, then at instant t_2, one of the series switches will go close to cut-off and the combined resistance of the series switch network will be large at instant t_2. This makes the tail current I_{tail} reach a very low value at instant t_2. At instant t_2, both I_p and I_n are at VDD. In other words, this is the instant at which the ISF is maximum for the VCO. By reducing the bias current at this instant t_2, the noise contribution due to tail current sources M_{t1} and M_{t2} is reduced. As the bias currents for the cross coupled transistors M_{gm1} and M_{gm2} are also low at this instant, the total noise contribution is reduced significantly. Two series switches are placed in parallel to get the series switch network so that both Q_p and Q_n see equal loading. Figure 3.3 shows a plot of tail current I_{tail} and the in-phase differential signal $I_p - I_n$. The tail current is minimum at the point at which in-phase differential output reaches a value 0 V, where the ISF is

maximum.

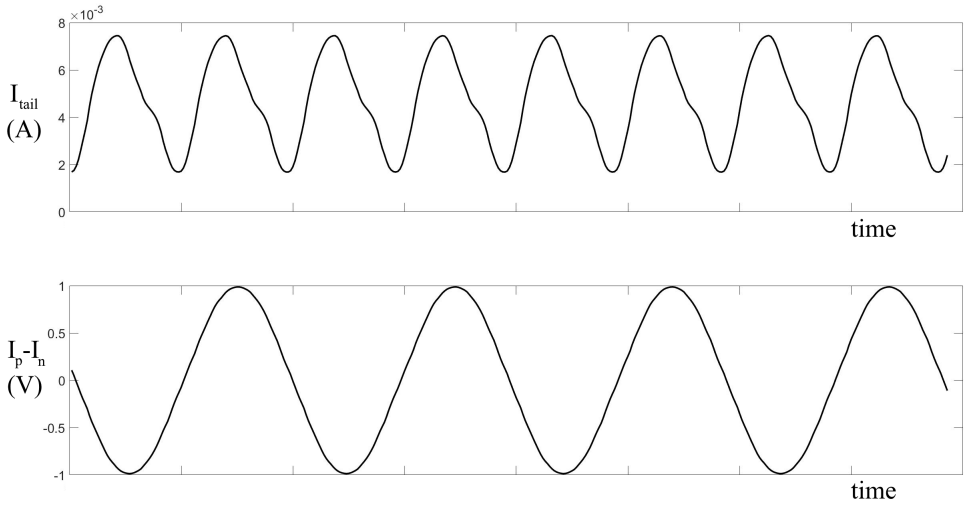

Figure 3.3: Plots of I_{tail} and in-phase differential output $I_p - I_n$ vs time

3.2 QVCO using an innovative coupling technique

The major problems in both P-QVCO and S-QVCO are the bimodal oscillation and the phase noise degradation because of coupling network. Superharmonic coupling addressed this issue by coupling through tail nodes either by using a transformer or a capacitor, as explained in Chapter 2. Transformers occupy too much area. In addition, such architectures using coupling through tail nodes assume that the VCO operates in the current limited regime so that the tail nodes aren't distorted and contain only the second harmonic component. In this thesis, a new architecture is proposed that could potentially solve the issue associated with bimodal oscillations without using the traditional coupling network. Consider the circuit show in Figure 3.4. This circuit has some interesting proporties. If an ideal tail current clipping, explained in Figure 3.1, is assumed, then Figure 3.4 can be simplified as shown in Figure 3.5. Though this is possible only if an ideal tail current clip-

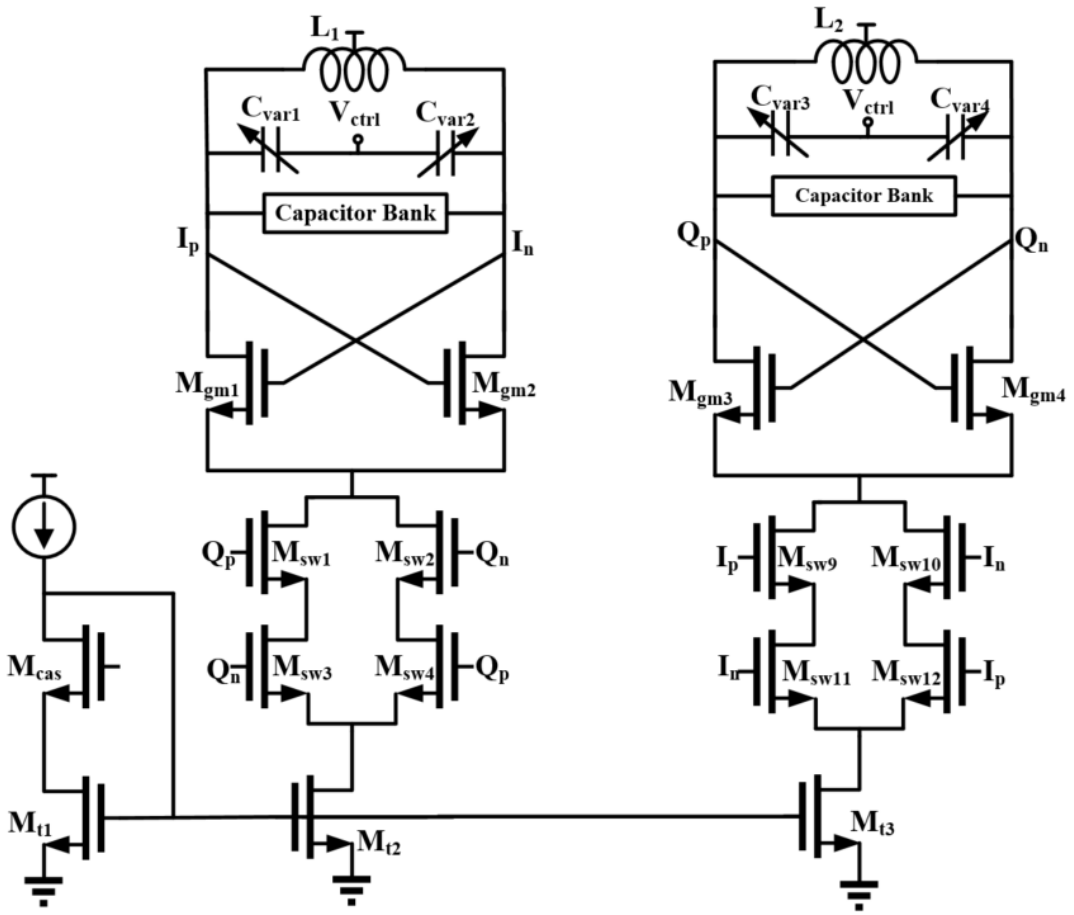

Figure 3.4: The proposed QVCO circuit with an innovative coupling network

ping network is considered, this helps in providing a basic insight into the circuit. SW_I and SW_Q model the series switches. If the implemented logic is assumed to be ideal, then the tail current gets injected into the I and Q circuits only at the zero crossings of $Q_p - Q_n$ or $I_p - I_n$ respectively. Consider a single VCO, as shown in Figure 3.6. Tail current is denoted by I_{tail} and this splits into two current signals $\frac{I_{tail}}{2} + \frac{\Delta I}{2}$ and $\frac{I_{tail}}{2} - \frac{\Delta I}{2}$ to the LC tank circuit based on $I_p - I_n$ values, as shown in the figure. Note that I_p and I_n denote the in-phase positive and negative voltage signals and shouldn't be confused with current I. The corresponding plots of current signals are shown in Figure 3.7. For the sake of

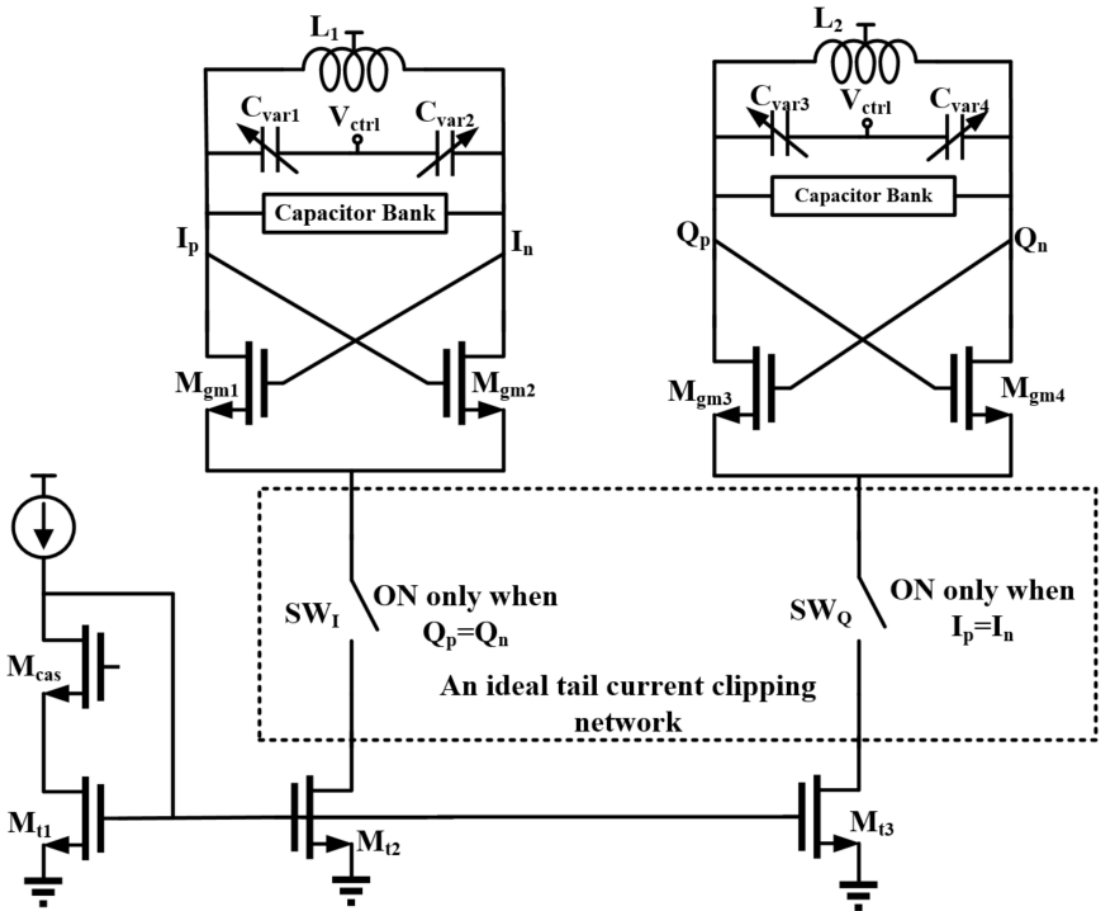

Figure 3.5: QVCO with an ideal tail current clipping network

argument, assume that both I and Q are in-phase. If they are in-phase signals, then at the instants where Q_p=Q_n, I_p is also equal to I_n. This means ΔI_{peak}, the differential current into the tank circuit, should be equal to zero. In other words, there is no differential current that gets injected into the tank circuit and the loop fails to oscillate. Intuitively, ΔI shown in the Figure 3.7 gets filtered by the tank circuit to obtain the output sinusoidal waveform. If ΔI_{peak} goes to zero, then the filtered output is also zero. If the phase difference between in-phase and quadrature signals is denoted by θ_d, as shown in Figure 3.8, then the differential peak current amplitude vs θ_d can be approximated as shown in the Figure 3.9. This plots looks similar to a half-sinusoid. As θ_d increases, differential

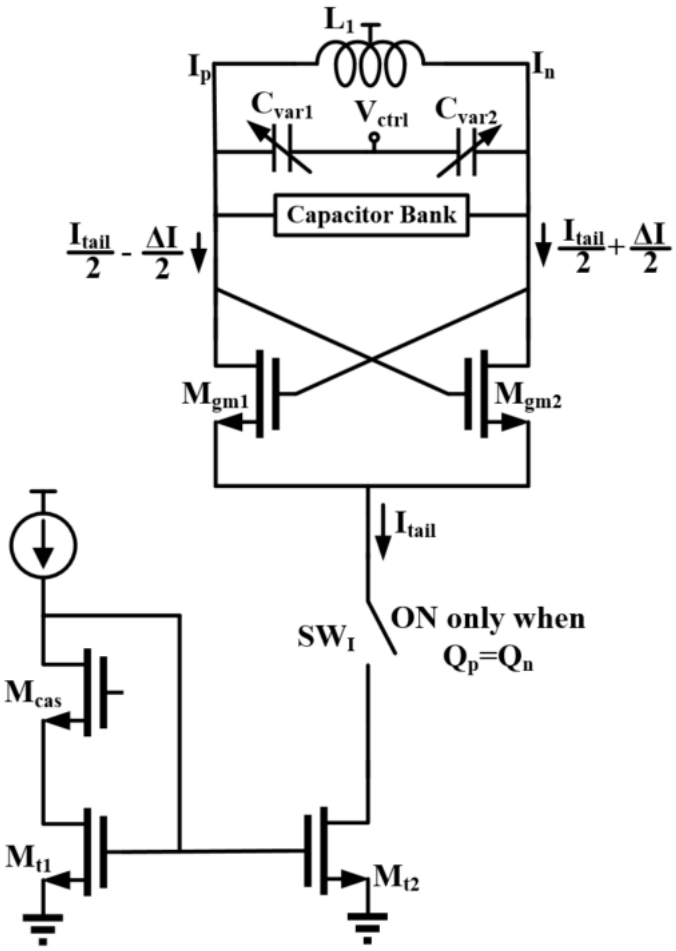

Figure 3.6: In-phase portion of QVCO with an ideal tail current clipping network

in-phase voltage $I_p - I_n$ at instants where Q_p=Q_n increases and the differential peak value ΔI_{peak} also increases. After some point, ΔI_{peak} should ideally saturate to I_{peak} because M_{gm1} or M_{gm2} should completely switch the current to one of the arms. Note that even beyond this point, ΔI_{peak} increases a little because of the inherent non-idealities in the MOSFETs and tail current source. Regardless of the shape of the plot of ΔI_{peak}, what matters is that the differential current that goes into the tank is maximum when I and Q are quadrature with respect to each other. This is very important for the understanding of this circuit. If the complete QVCO shown in Figure 3.4 is considered, the plot of loop gain for

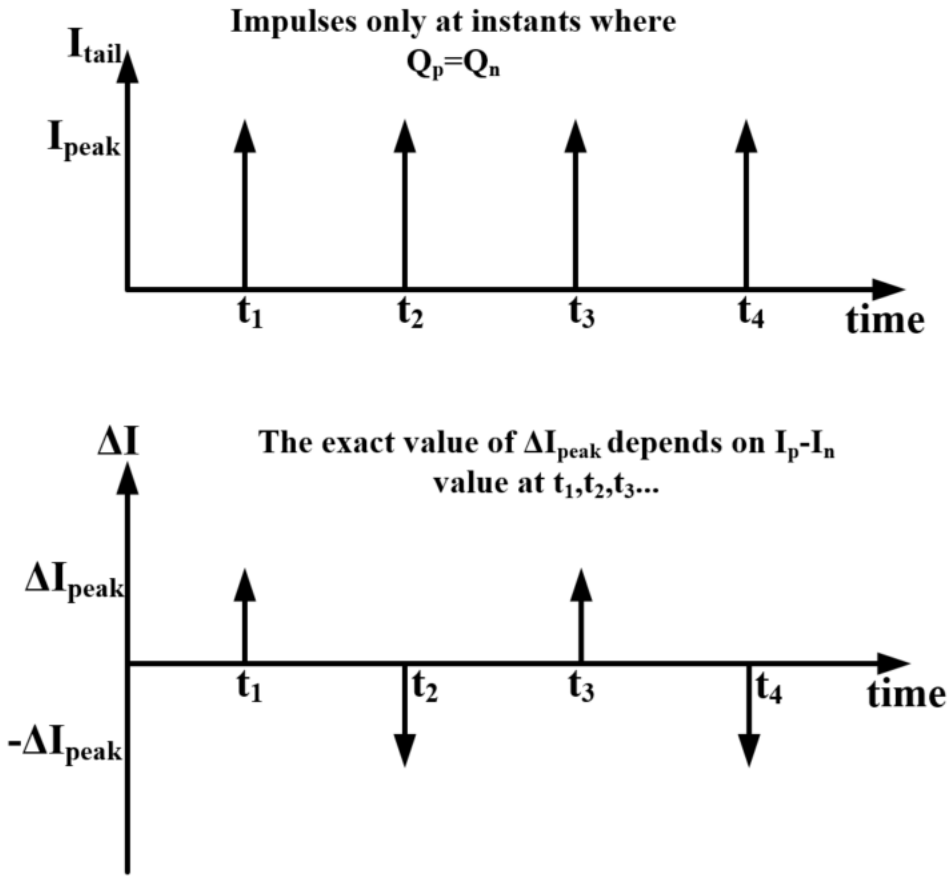

Figure 3.7: Plots of tail current and differential current into the tank circuit vs time

the loop, which includes both I and Q, vs θ_d will have a shape that looks approximately similar to ΔI_{peak} vs θ_d. This is stepper than the Figure 3.9, as there are two VCOs and they total loop gain includes the multiplication of shapes of two ΔI_{peak}s.This is shown in Figure 3.10. This helps by further strengthening the stable point of 90° phase difference between I and Q. The stable point of oscillation is when the loop gain is maximum, which in this case corresponds to a phase difference θ_d of $\frac{\pi}{2}$. The other possible solutions that correspond to a phase difference θ_d not equal to $\frac{\pi}{2}$ are suppresed. In other words, the stable point solution at $\frac{\pi}{2}$ sustains oscillations when the total large signal loop gain is equal to 1 based on Barkhausen criteria, and the large signal loop gain is less than 1 for other solu-

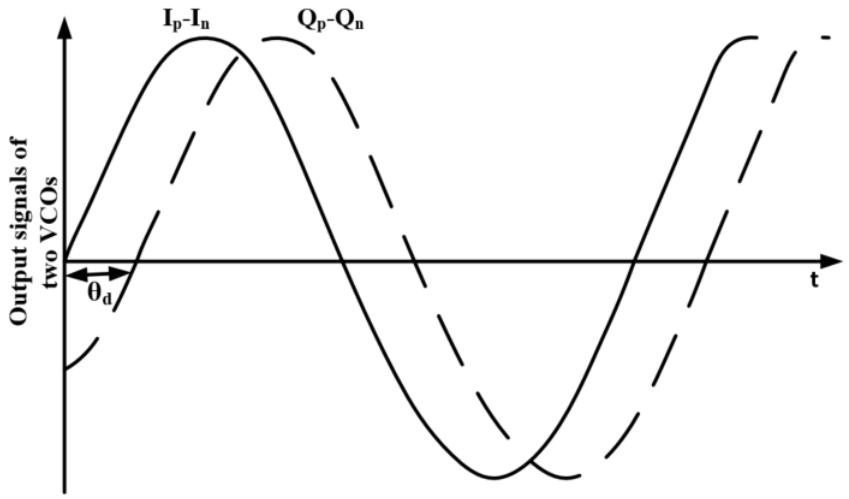

Figure 3.8: I and Q signals with a phase difference θ_d

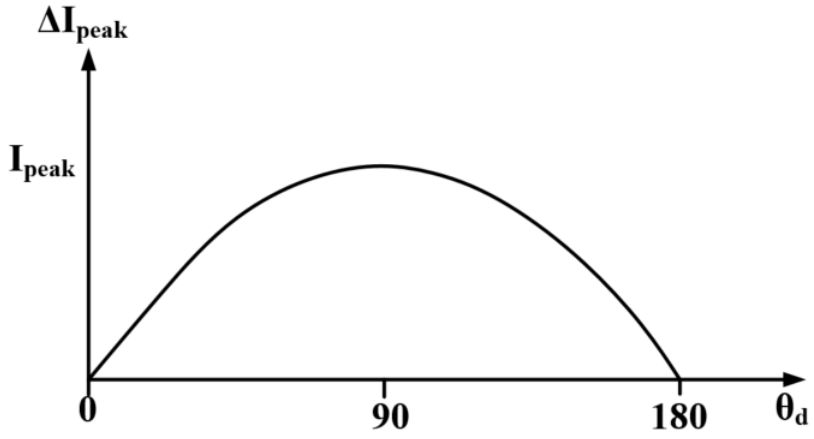

Figure 3.9: Differential current into the tank circuit vs θ_d

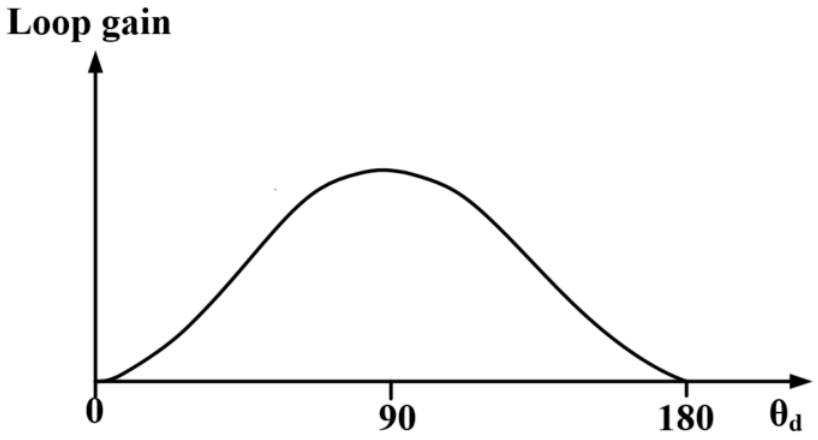

Figure 3.10: Loop gain of the QVCO vs phase difference θ_d

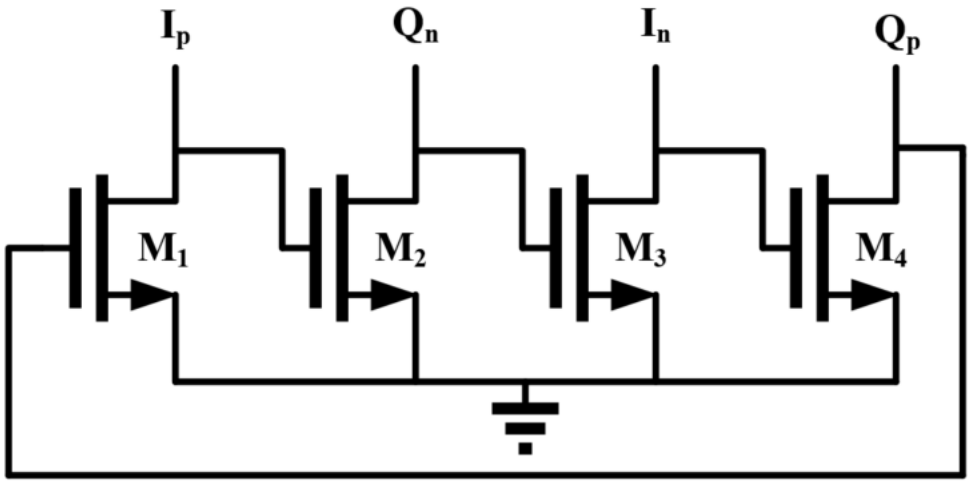

Figure 3.11: Weak transistors that help in resolving the ambiguity in the sign of the phase difference between I and Q

tions. Therefore, a quadrature VCO is obtained without any using the traditional parallel or series coupling network. Even in the presence of non-idealities of switches, the QVCO settles at the point at which the loop gain is maximum, which always corresponds to a θ_d of $\frac{\pi}{2}$ as long as the two VCOs are matched. Since this is a symmetric circuit, there is an ambiguity on the sign of phase difference between I and Q i.e. it's not quite clear as to whether I lags or leads Q. This issue can be resolved by using a structure discussed in 2.11, shown in Figure 3.11. The transistors M_1 to M_4 are weak and they don't draw that much current. They are just present to resolve the ambiguity in the direction of the phase difference.

3.2.1 Advantages

The advantages of the proposed architecture is explained as follows.

(i) Elimination of coupling network means that there are no bimodal oscillations and any additional phase noise due to the coupling network. This should improve the phase noise performance by a considerable amount, as the Q factor is maximum at the resonant frequency. The noise due to series switches is negligible. This is explained in Figure 3.12 [1]. When Q_p is higher than Q_n, M_{sw3} and M_{sw2} are OFF and prevent the noise currents of M_{sw1} and M_{sw4} from entering the LC tank circuit. Similarly, the noise is negligible when Q_p is lower than Q_n. The case when $Q_p = Q_n$ is not a big issue because that's when ISF is minimum and the noise due to the switch network at that instant should have very negligible effect.

(ii) Unlike superharmonic coupling methods discussed before, there is no need to couple two VCOs through tail nodes and hence the assumption of current-limited regime is not required here. The tail nodes, in addition, don't have a huge swing, whereas in the proposed structure the inputs to the switches are the outputs of the QVCO, which have huge swings. The proposed structure doesn't make use of any transformers or any tail node

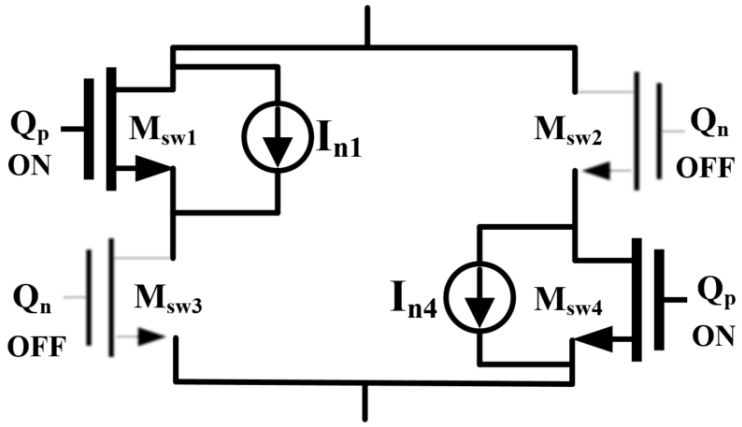

Figure 3.12: The noise due to series switches assuming when Q_p is high and Q_n is low

coupling capacitors. Note that this architecture should not be confused with S-QVCO discussed before. Though the coupling transistors are in series in S-QVCOs, they are G_{mc} cells as opposed to non-linear switches. S-QVCO also has an issue of allocating headroom for these series transistors, whereas in the proposed structure the switches don't consume that much hearoom if their resistances are small enough. This makes it an attractive solution for low supply voltage technology process nodes.

(iii) One of the important features of this structure is that it inherently injects the tail current into the LC tank circuit when the ISF is minimal, as explained in the section on tail current clipping. By doing so, the phase noise contribution due to tail transistor and other transistors can be reduced considerably.

(iv) No additional current is required for coupling two VCOs. The proposed architecture just re-uses or shapes the I_{tail} so as to obtain quadrature outputs. This reduces the power consumption.

(v) There are no coupling transistors and hence the mismatch due to coupling transistors is eliminated completely. The effect of mismatch of the switches is also negligible compared to mismatch between coupling networks using G_{mc} transistors. As explained

later in this chapter, the phase error due to mismatch in the proposed architecture is ideally lower than that of the traditional P-QVCO.

3.3 Non-idealities

The non-idealities that are possible in the proposed architecture and the effects of those are analyzed in this section. Even if the series switches aren't ideal and have a non-zero ON resistance and ON duration (I_{tail} in Figure 3.7 is spread throughout instead of impulses), it's easy to observe that the loop gain is still maximum at $\theta_d = \frac{\pi}{2}$. This ensures that the oscillators still operate in quadrature. Simulation results indicate that the phase shift between I and Q is not disturbed because of this non-ideality. The architecture relies on the instants at which the tail current gets injected into the LC circuit. Even if I and Q are in quadrature, it is possible that there could be some delay through the switches and cross-coupled transistors M_{gm1} and M_{gm2}. Consider the structure shown in Figure 3.13. Here the delays through I and Q paths are modeled by I_{delay} and Q_{delay}. As long as the two circuits are symmetric, it's safe to assume that $I_{delay} = Q_{delay}$. This is a valid assumption if the mismatch effects aren't considered. It can be shown that even in the presence of I and Q delays, the outputs are still quadrature with respect to each other as long as I and Q delays are matched and the delays are not huge. If I and Q aren't in quadrature as shown in Figure 3.14, then Q-phase sampling points t_1 and t_2 are at their peak values, but I-phase sampling points t_3 and t_4 aren't at the peak values. Effectively, the total loop gain is determined by the multiplication of both these values and they tend to be low if I and Q aren't off by 90°. In other words, the loop gain is still maximum at 90° and I and Q operate in quadrature even in the presence of delay. This was observed in simulations as well. An issue that was observed was that if the delay was large enough, as shown in Figure 3.15, it could be possible for the loop gain to go maximum at 0° phase shift between I and Q because the sampling points are such that they are at the peak values if I and Q signals

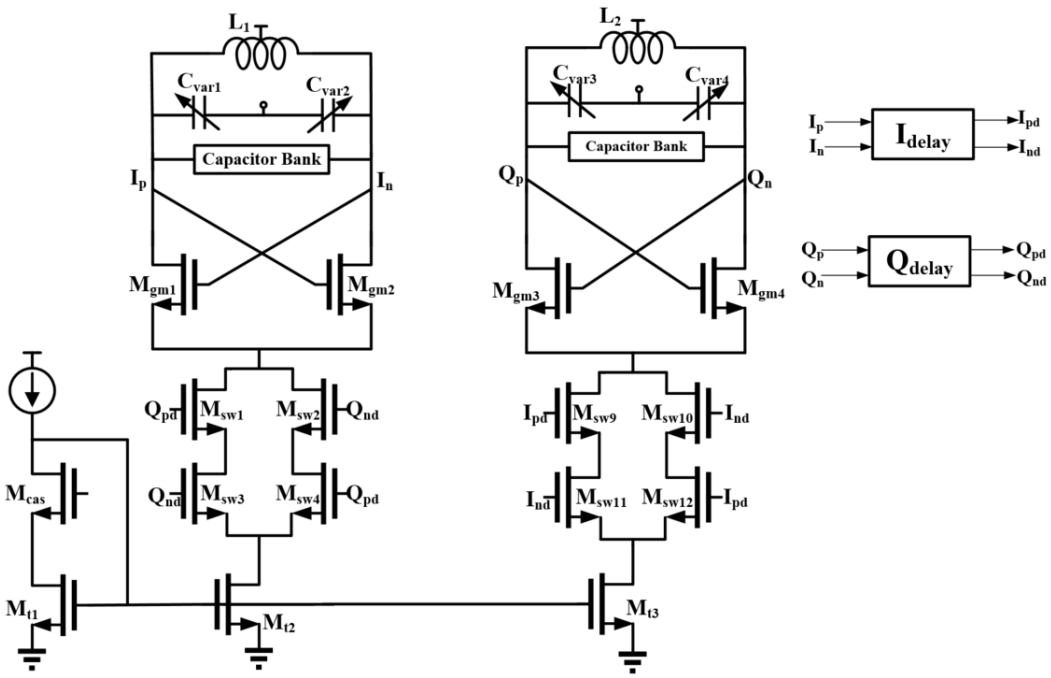

Figure 3.13: Effect of delay from I and Q to input of switches

are close to in-phase. In this case, it was observed that the VCOs operate in-phase rather than quadrature phase. This delay required is found to be large, and this specific case is not a great concern. The additional delay required to obtain this solution increases as the frequency of oscillation reduces. Therefore, the QVCO operates in quadrature even in the presence of delays through I and Q paths, as long as the two VCOs are symmetrical with respect to each other.

3.4 Effect of mismatch

The proposed architecture has a strong preference for 90° phase shift where the loop gain is maximum. However, in the presence of mismatch in resonant frequencies of two tanks for example, other constraints need to be taken into account. Consider the traditional P-QVCO discussed before. Assume that there is a mismatch in resonant frequencies of the two VCOs. As explained in [9], the phase error due to this mismatch is determined by Eq.

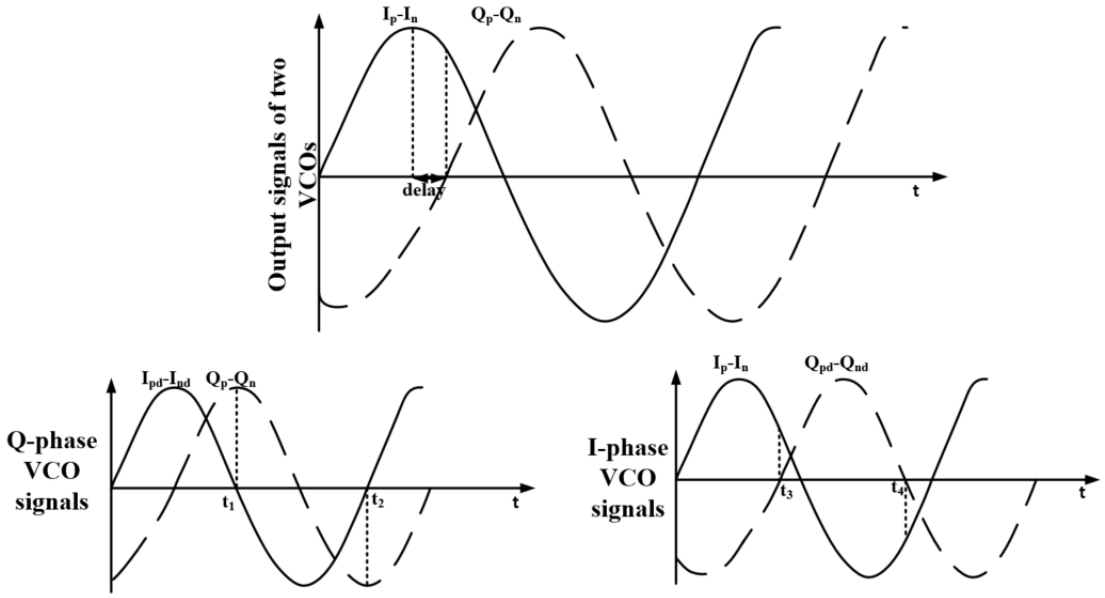

Figure 3.14: Sampling points in I and Q VCOs in case I and Q are not in quadrature because of a small delay

3.1,

$$d\phi = \left(1 + \frac{1}{m^2}\right).\frac{\theta_m}{2} \approx \frac{Q}{m^2}.\frac{d\omega}{\omega_{osc}} \tag{3.1}$$

In Eq. 3.1, $d\omega$ is the mismatch in the resonant frequencies and θ_m is the additional change in the angle between the voltage and current vectors of the LC tank circuit due to offset from the resonant frequency. θ_m can be determined from Figure 2.8 for a given offset in the frequency from the resonant frequency. Q is the quality factor of the LC tank circuit, m is the coupling coefficient defined before, ω_{osc} is the center frequency of oscillation and $d\phi$ is the phase error with respect to the ideal 90° phase difference between the two VCOs. The main issue with P-QVCO is that the coupling factor m is usually less than 1 to reduce the effect of bimodal oscillations. Generally, m is equal to 0.2 to 0.25 [8]. If $m = 0.25$, then the phase error $d\phi$ in Eq. 3.1 is more than θ_m. In other words, in order

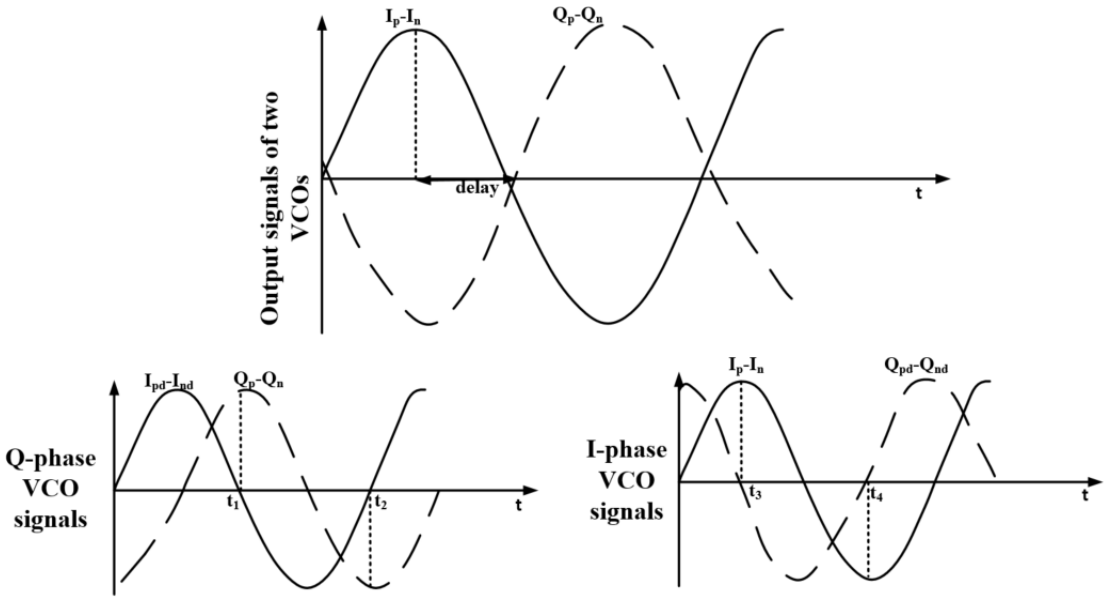

Figure 3.15: Sampling points in I and Q VCOs in case I and Q are not in quadrature because of a large delay

to correct for θ_m change, the loop has to have a phase error more than θ_m. If $\theta_m = 0.5°$ and $m = 0.25$, then phase error $d\phi$ is $4.25°$. The phase error $d\phi$ is 8.5 times more than the original θ_m. Therefore, there is a huge need for reducing θ_m by having proper matching. Consider the proposed architecture. Figure 3.5 is redrawn in Figure 3.16 for the ease of explanation. If there is a mismatch in the resonant frequency by $d\omega$, going by the previous argument, there will be an additional phase change $d\theta$ needed between the voltage and current vectors of the LC tank circuit. If ideal impulses in tail current explained in Figure 3.7 is assumed, then it's quite obvious that for this $d\theta$ correction, the phase error between the two VCOs $d\phi$ should also be equal to $d\theta$ and it is the only possible solution, as shown in Figure 3.17. Here ΔI is the differential current flowing into the LC tank circuit. In this case, $d\phi_1$=$d\theta$. In other words, this is equivalent to having $m = 1$ in Eq. 3.1 while not having any bimodal oscillation issue. Therefore, the proposed architecture is superior in terms of phase accuracy compared to P-QVCO. It was assumed that the tail current is

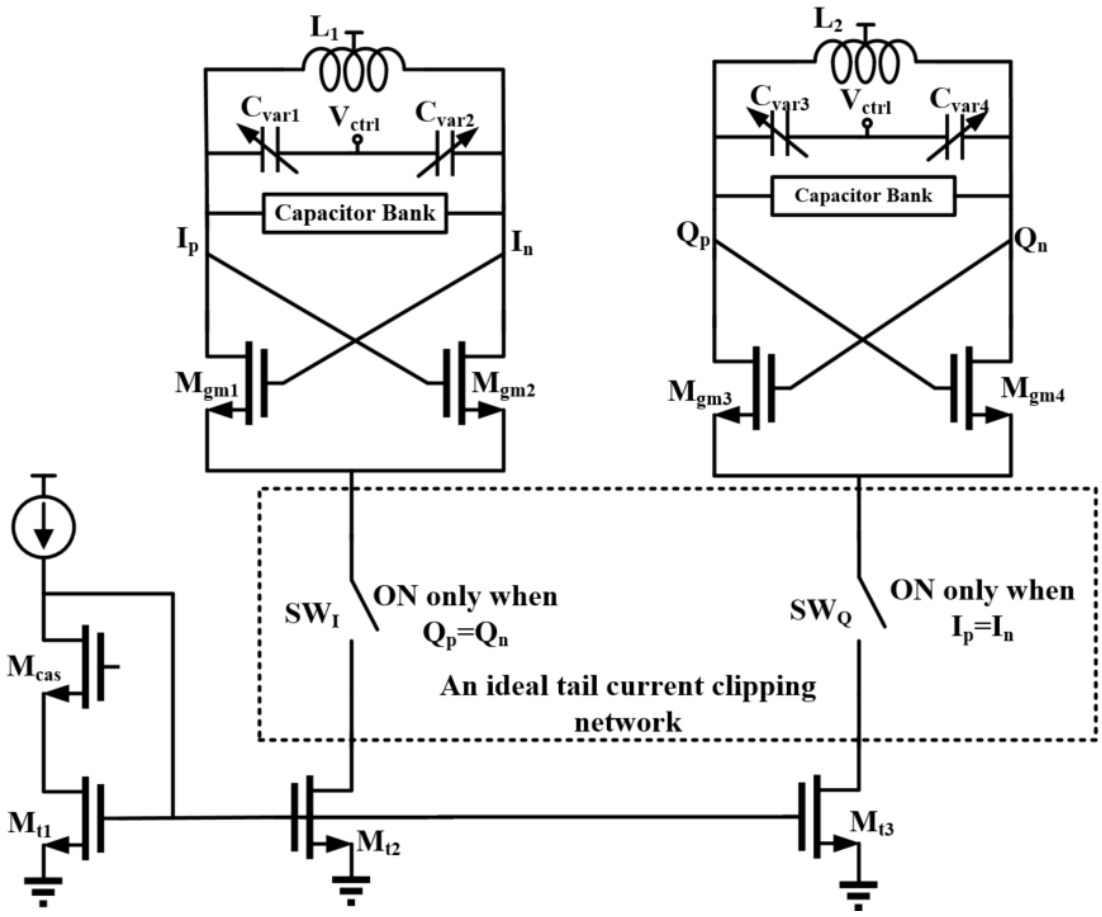

Figure 3.16: QVCO with an ideal tail current clipping network. Assume that there is a mismatch in the resonant frequencies.

in the form of impulses. This is only an ideal scenario. The sensitivity of the QVCO to mismatches depends on the shape or slope of the tail current waveform. This depends on the ON-time of the switches M_{sw}s. In general, the current waveform looks like the one shown in Figure 3.18. Note that the tail current is no longer in the form of impulses. In order to compensate for this non-ideal I_{tail} waveform, the differential current into the tank and hence the output signals $I_p - I_n$ get shifted by $d\phi_e$. The phase error $d\phi_2$ is equal to $d\theta + d\phi_e$. An ideal tail current shape is obtained as the output swing increases. This is because the switches enter into the cut-off region quickly as the swing increases.

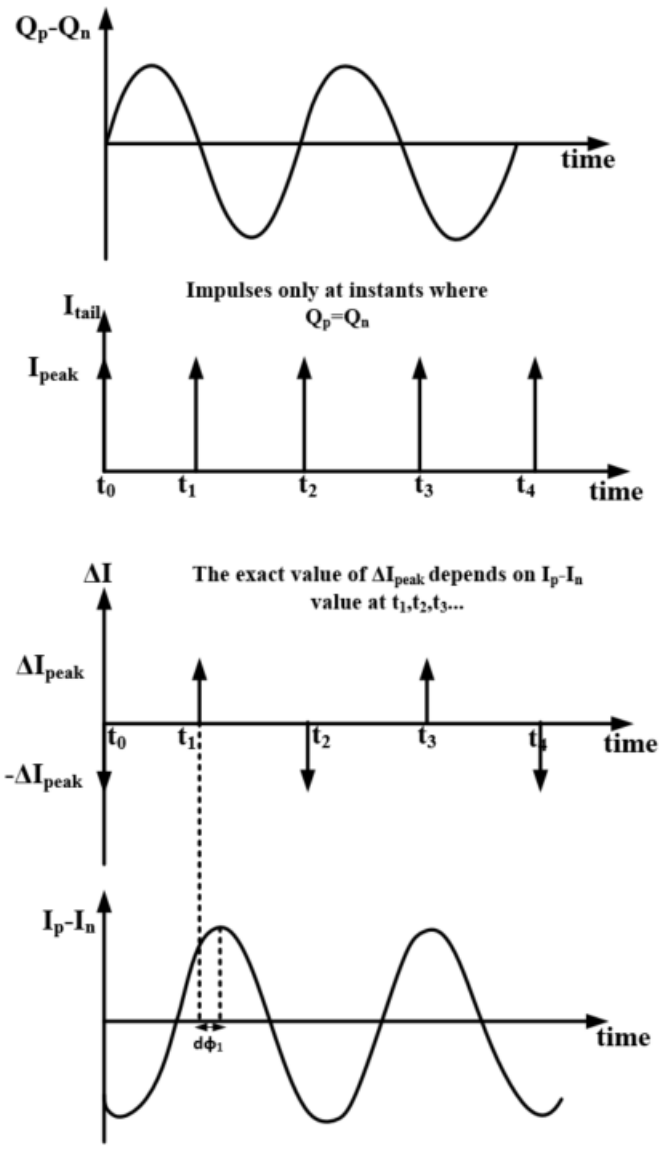

Figure 3.17: Plots of Quadrature signal, tail current, differential current into LC tank and In-phase signal assuming ideal switches

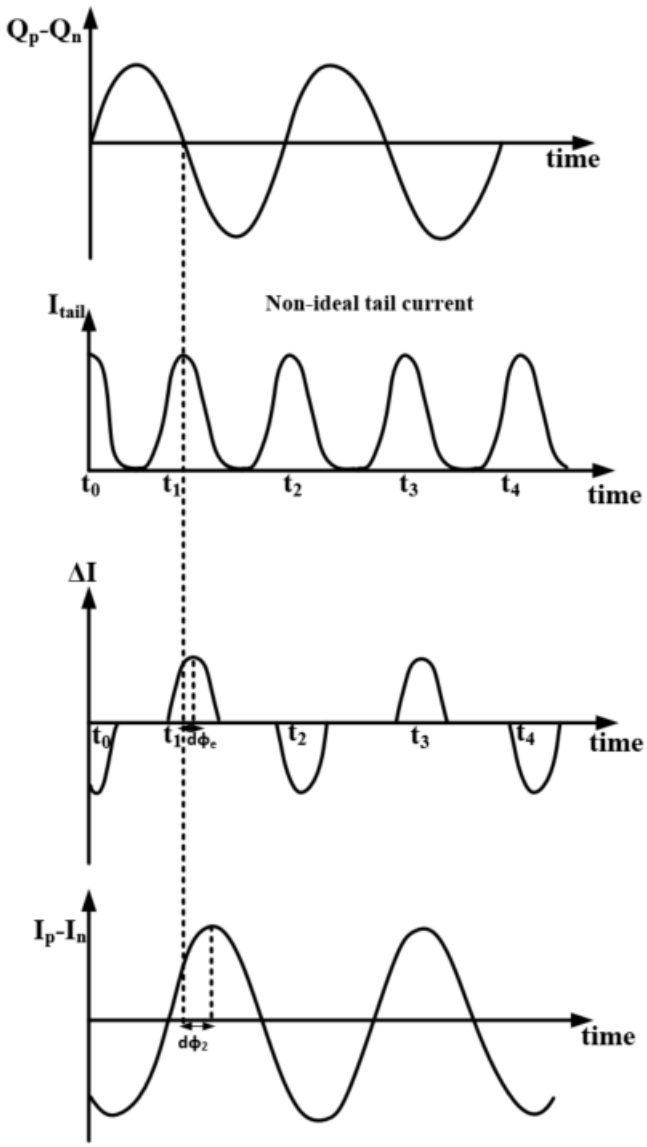

Figure 3.18: Plots of Quadrature signal, tail current, differential current into LC tank and Inphase signal assuming real switches

As the output swing increases, $d\phi_e$ reduces and hence the phase error also reduces. It was observed on simulation and during measurement that increasing the amplitude of the swing improves the phase accuracy. This is not a characteristic of a P-QVCO. Simulation results indicate the phase errors due to P-QVCO and the proposed architecture are nearly equal.

3.5 Top level Diagram

The top level block diagram is shown in Figure 3.19. The output buffers used are

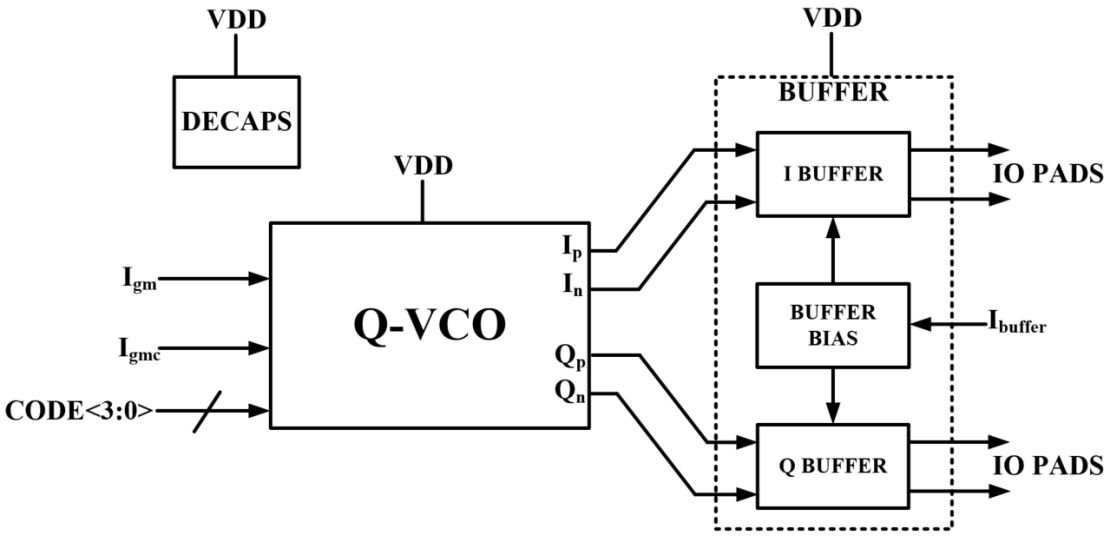

Figure 3.19: Top level block diagram of Q-VCO.

based on CML logic. The CML buffer used is shown in Figure 3.20. The resistance R_D is chosen so that the single ended impedance seen looking into the CML buffer is close to 50 Ω, as the output goes to the pads and finally to the oscilloscope via PCB traces. An unit capacitor bank circuit is shown in Figure 3.21. In this circuit, C_{mom} is the Metal-on-Metal (MOM) capacitor. M_{sw} is the main switch transistor that is large. M_1 and M_2 are weak pull down transistors that ensure that the intermediate nodes V_1 and V_2 are at 0 V DC. This

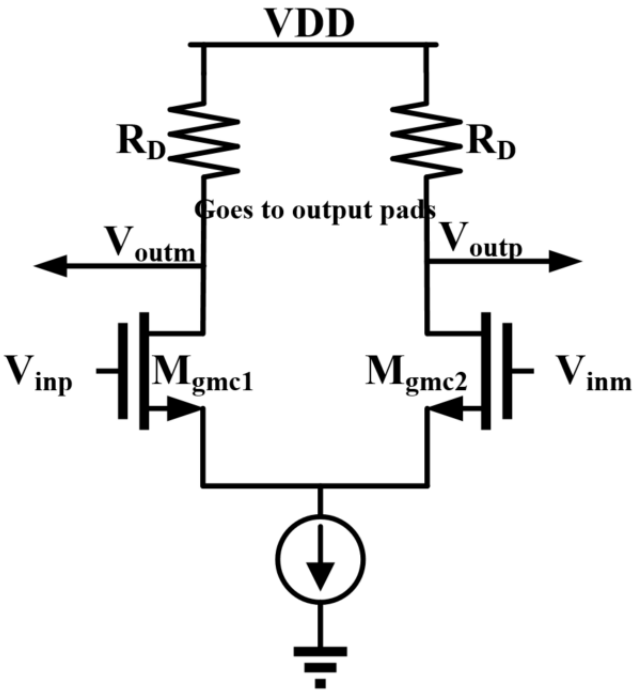

Figure 3.20: CML Buffer.

helps in reducing the resistance of M_{sw} and hence improves Q factor of the capacitor bank circuit. Similarly, R_p resistors are large resistors that pull up the nodes V_1 and V_2 to VDD when Enable signal EN is 0 V. This ensures that M_{sw} is always OFF when EN is 0 V. The capacitor bank consists of four such units that are controlled by inputs CODE<3:0> shown in Figure 3.19. This makes the resonant frequency tunable from 3 GHz to 6 GHz based on the results obtained on simulation. The measured tuning range was from 4 GHz to 5 GHz due to extra parasitics and inaccuracies in the modeling of inductors.

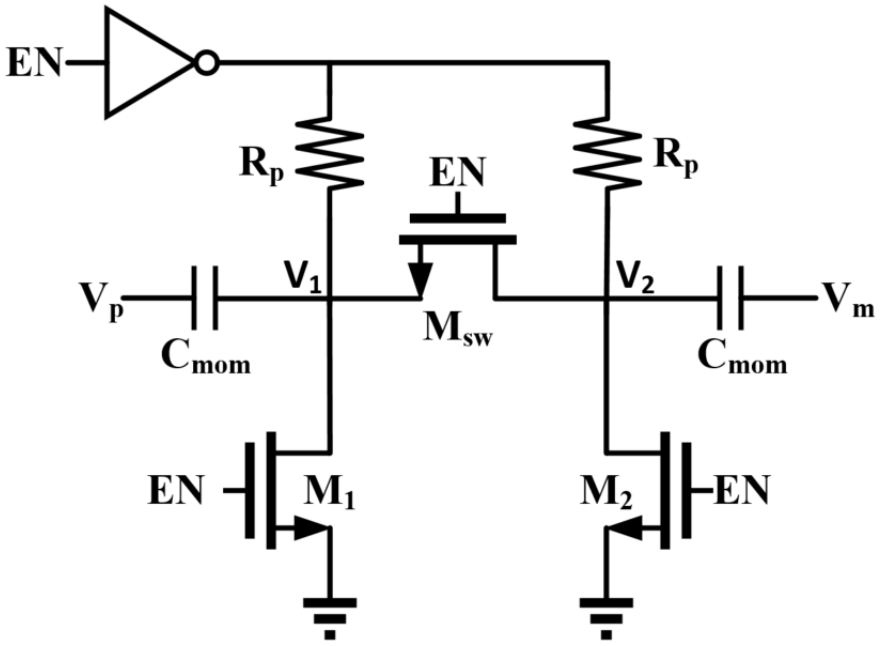

Figure 3.21: An unit capacitor bank circuit.

4. SIMULATION AND MEASUREMENT RESULTS

This chapter is organized as follows. First, inductor design simulations are reported. This is followed up by simulation and measurement results.

4.1 Inductor Design

Designing the inductors was an important part of the thesis, as the Q factor of the inductor plays a vital role on the phase noise value. The main challenge in designing the inductor was on obtaining a decent Q factor in the 40nm technology node that had only 8 Metal layers with no Ultra Thick Metal layer (UTM) for the inductor. There was no access to the foundry inductors so the inductors had to be designed using an Electromagnetic (EM) simulation tool. SONNET software was used for this purpose.There were only 2 Thick Metal layers M7 and M8, which were also used for supply and ground nets. There are two issues because of this. First, the ground capacitance that M7 and M8 see is more than what an UTM would see. This results in reduction in the resonant frequency. Also, the resistivity of M7 and M8 is larger than that of UTM, as UTM layers are thicker. Finally, since M7 and M8 are also used for supply and ground nets, the usage of supply and ground nets gets restricted in some places. For these reasons, the design of inductors became a challegining part of the project and took several iterations. If there is access to UTM layer or few more thick metal layers, it is possible to obtain a better phase noise FOM than what's reported in this thesis. An image of the schematic is shown in Figure 4.1 along with the dimensions. In order to increase the resonant frequency, the number of turns were reduced to 2 so as to minimize the coupling capacitors between two adjacent turns. A size of 20 μm width was chosen to minimize the resistance. Note that increasing the width reduces the resonant frequency, as the capacitance to the ground increases. There is a trade-off and an optimum value is chosen. Based on these constraints, the size of

the inductors was chosen to obtain the required inductance value of around 1 nH. The 3-Dimensional view is shown in Figure 4.2. In order to consider the effect of coupling

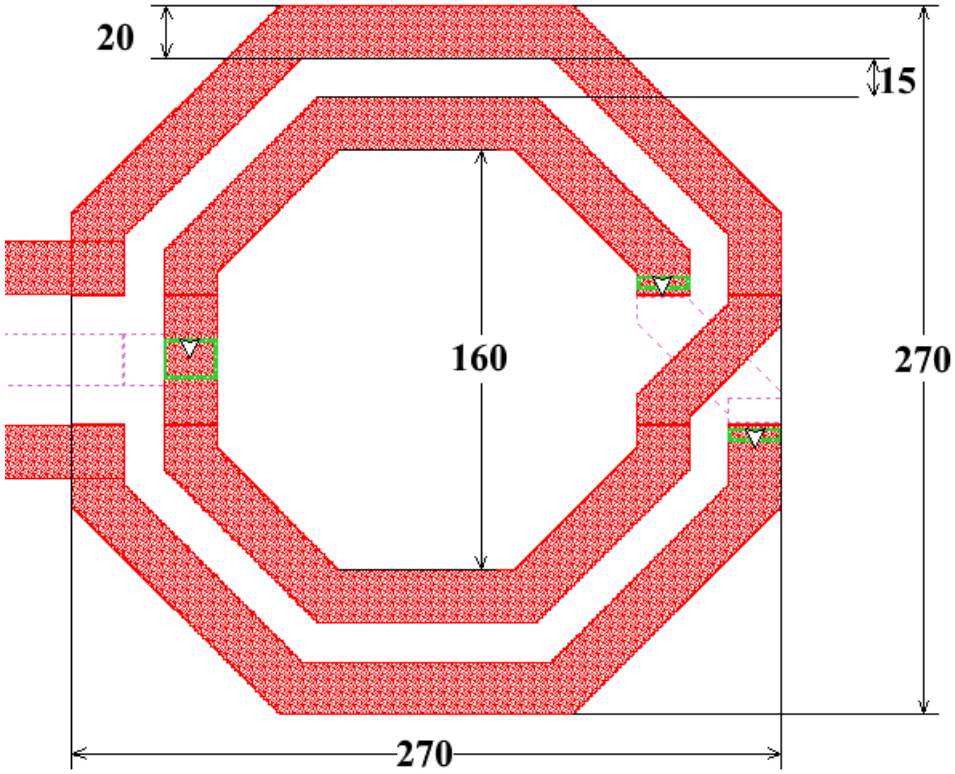

Figure 4.1: Inductor along with dimensions. The dimensions are in μm.

between two inductors, while simulating for the Q factor, both the inductors are considered in the EM simulation and the s-parameter was extracted for SPECTRE simulations. The layout for this test setup is shown in Figure 4.3. A distance of 730 μm indicates the distance between the two inductors on the layout of Q-VCO. This models the effect of coupling between the two inductors. EM simulations were made using SONNET tool for obtaining the Q factor of inductors. The plot of inductor value and Q factor vs frequency

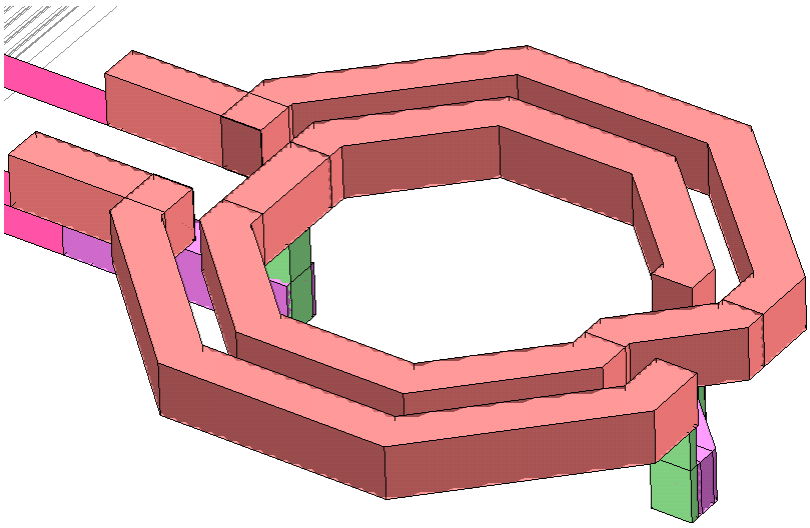

Figure 4.2: A 3-Dimensional view of the inductor.

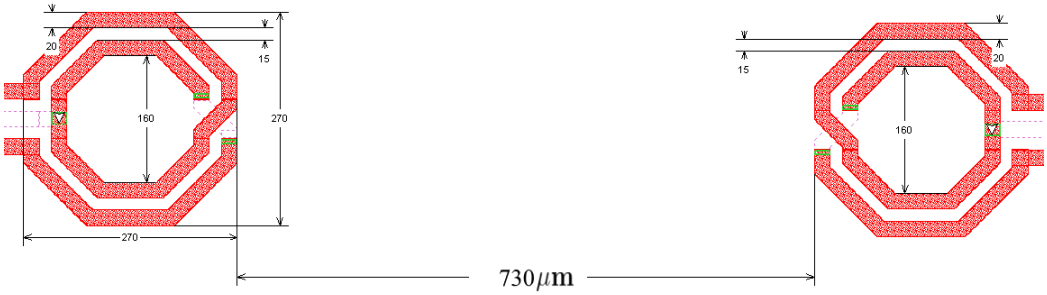

Figure 4.3: Test setup layout for simulation of the Q factor of the inductors.

range is shown in Figure 4.4

4.2 QVCO results

The design was completed in the CMOS 40nm technology. Inductors were designed using Metal layers M8 and M7 of the technology because access to higher metal layers wasn't available. If the inductors are designed using higher metal layers or ultra-thick metal layers, an FoM (Figure of Merit) more than the number reported in this thesis can be obtained. A differential center-tapped inductance of about 1nH was designed. It was ob-

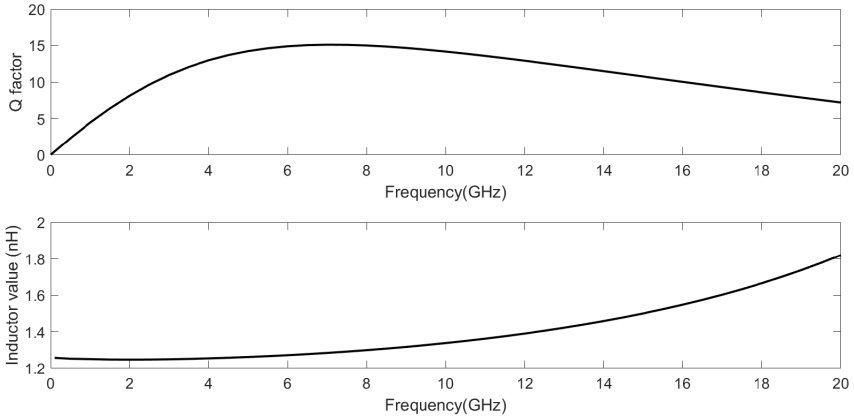

Figure 4.4: Plot of Q factor and inductance value vs frequency.

served that in order to get satisfactory Q factor, the inductance value couldn't be increased more than this due to the self-resonant frequency reduction arising from the increase in the coupling capacitors from M8 and M7 metals to ground. Increasing the inductance on the other hand will help in reducing the power consumption for the same output swing and hence will improve the FoM. This has a Q factor of approximately 10 at 3GHz and 15 at 6 GHz. First the phase noise plot of the proposed technique with tail current clipping is compared with the phase noise plot of the traditional P-QVCO circuit without any tail current clipping. The phase noise plot is shown in Figure 4.5. Simulation results indicate an improvement of around 4 to 5 dB in the phase noise response. The plot of phase noise vs frequency is shown in Figure 4.6. The conventional Figure of Merit (FoM) for any VCO is defined as,

$$FoM = 20log\left(\frac{\omega_{osc}}{\Delta\omega}\right) - 10log(L(\Delta\omega)) - 10log(P\,mW). \tag{4.1}$$

In equation 4.1, ω_{osc} is the oscillation frequency, $\Delta\omega$ is the offset at which phase noise is measured, $L(\Delta\omega)$ is the phase noise value in dBc/Hz, P is the power consumption of the circuit in mW. The power consumption of the proposed architecture is around 11 mW.

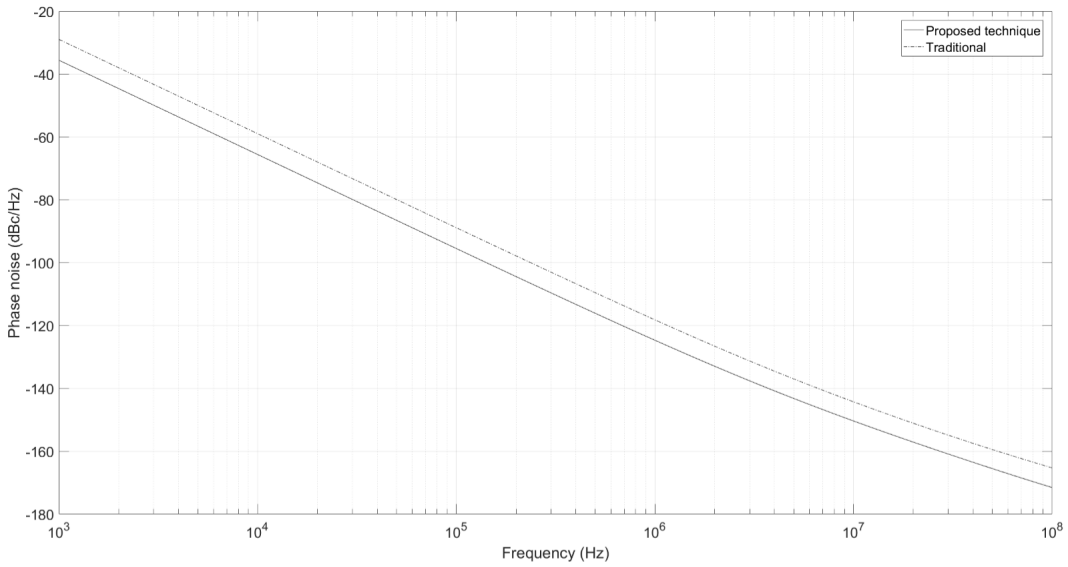

Figure 4.5: Simulated phase noise plot for the proposed technique with tail current clipping and the original QVCO for a 6 GHz output.

Based on Figure 4.6, it can be observed that the phase noise is around -123 dBc/Hz for a 6 GHz output signal and -140 dBc/Hz for a 3 GHz output signal at 1 MHz offset. This corresponds to an FoM of 188 dBc/Hz for 6 GHz output and an FoM of 198 dBc/Hz for 3 GHz output. The plot of frequency sweep vs varactor voltage for all capacitor bank codes is shown in Figure 4.7.

4.2.1 Effect of mismatch

Since in the proposed architecture no parallel or series coupling network is required, the mismatch due the coupling network is completely eliminated. The effect of mismatch due to the resonant frequencies of the two VCOs is considered here. As mentioned before, the phase error due to mismatch in the resonant frequency depends on the amplitude of the output signals, which is proportional to the tail current. It was observed that increasing the tail current was reducing the phase error. Phase error is observed for 0.5% mismatch in the resonant tank frequencies of the two VCOs for various values of tail currents of the

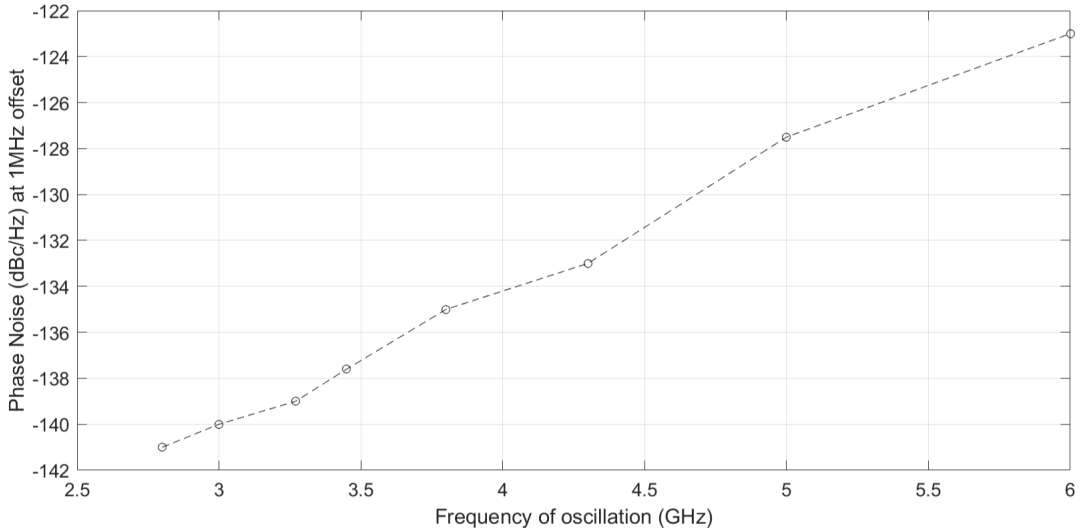

Figure 4.6: Simulated phase noise at 1 MHz offset for the output signal vs output frequency.

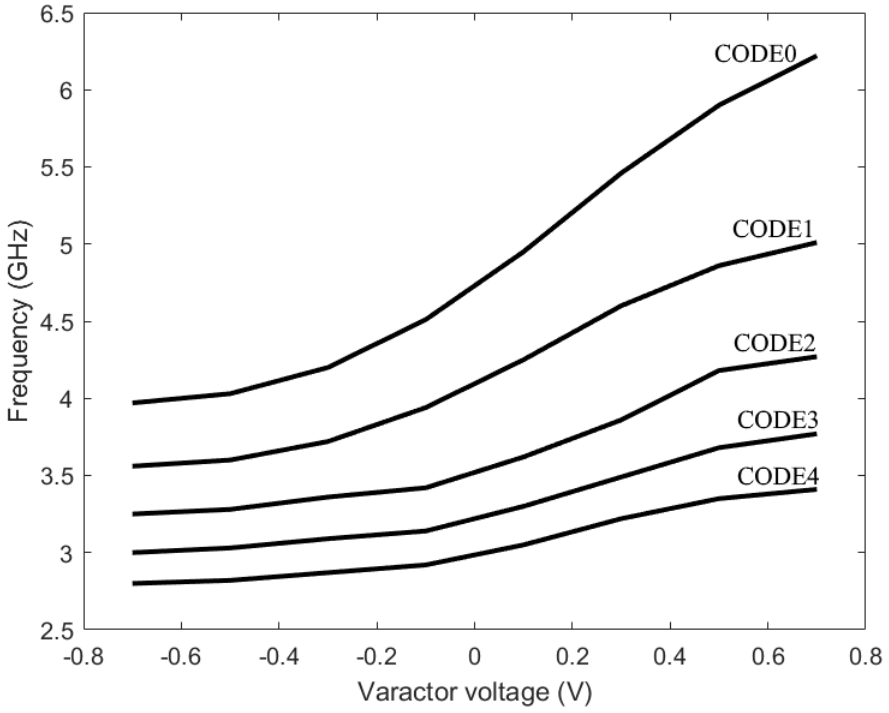

Figure 4.7: Simulated tuning range of the proposed QVCO.

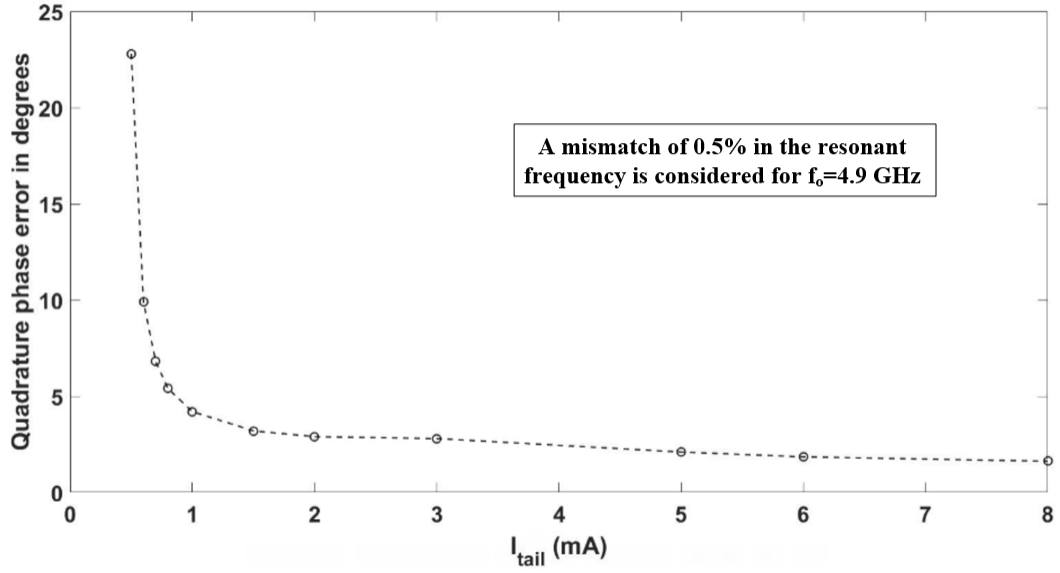

Figure 4.8: Simulated effect of average value of I_{tail} on mismatch vs frequency. A mismatch of 0.5% in the resonant frequency is assumed.

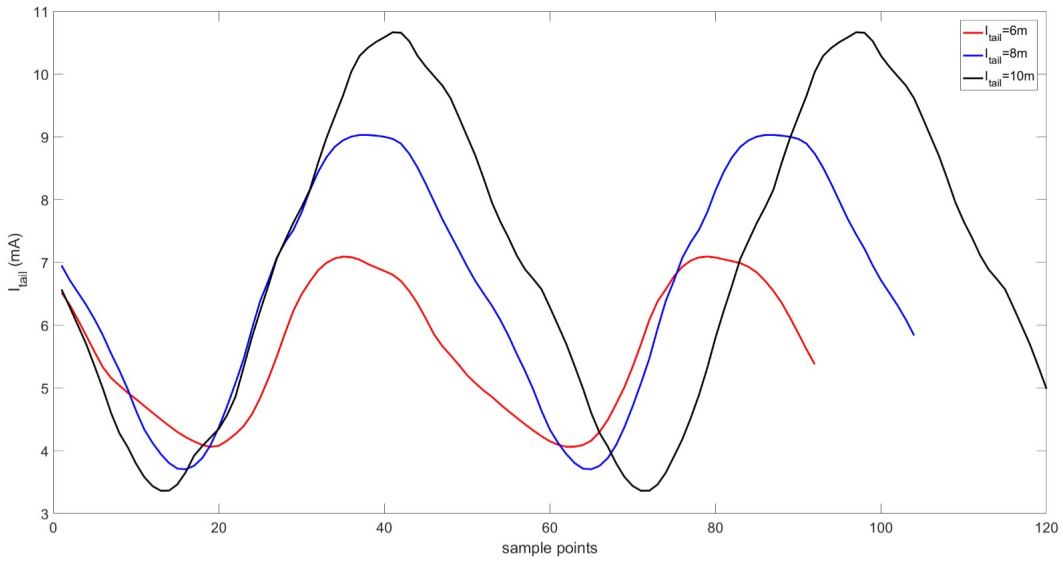

Figure 4.9: Simulated effect of average value of I_{tail} on shape of I_{tail}. A mismatch of 0.5% in the resonant frequency is assumed.

QVCO for a 4.9 GHz frequency. This is shown in Figure 4.8. The ratio of maximum to minimum value of I_{tail} increases with increase in average value of I_{tail} because of increase in the output swing and thereby improving the switching operation. This helps in reducing the sensitivity to non-idealities. The change in shape of I_{tail} with increase in the average value of I_{tail} is shown in Figure 4.9. As I_{tail} increases, the ratio of maximum to minimum value increases which makes the loop gain plot narrower.

4.3 Measurement Results

The chip was fabricated in the 40nm CMOS process. The chip micrograph is shown in Figure 4.10. The test-set up for measuring phase noise and phase accuracy is shown

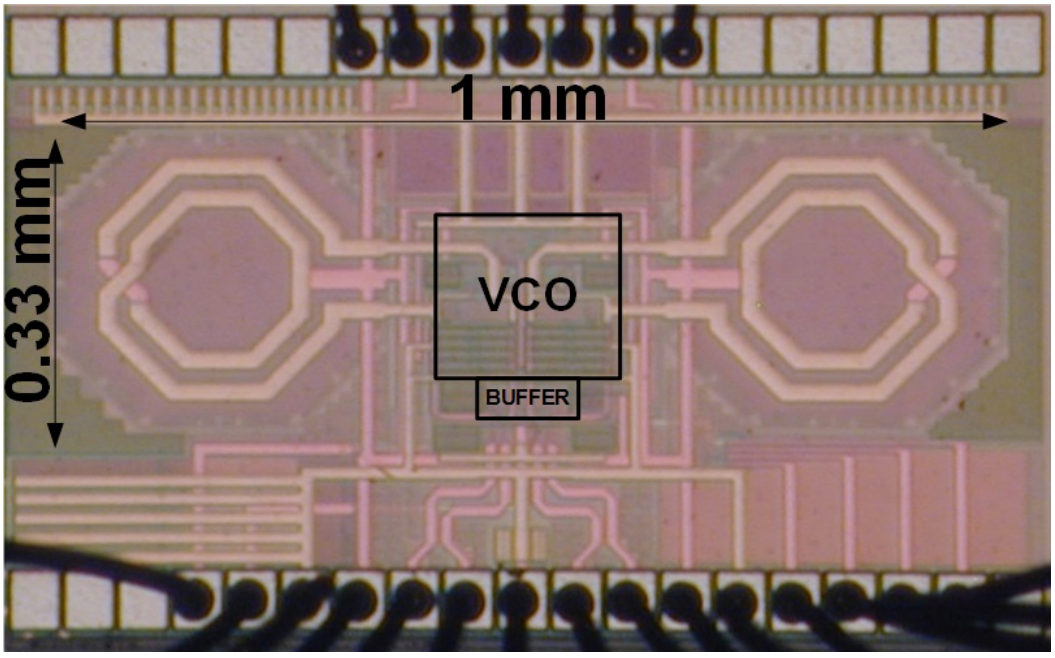

Figure 4.10: Micrograph of the chip.

in Figure 4.11. Short SMA cables each of 1 ft length were used to measure quadrature accuracy to reduce mismatches between I and Q. A hyrbid coupler was configured as a

balun to convert differential signals to single-ended in order to measure phase noise on the spectrum analyzer. With the tail bias current I_{gm}=5 mA, the chip was measured to

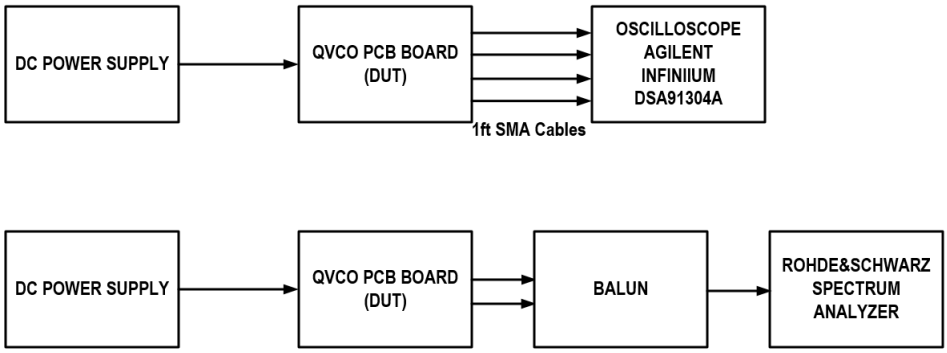

Figure 4.11: Test setup for measuring phase accuracy and phase noise

be tunable from 4 GHz to 5 GHz. Though the circuit works from 3 GHz, the measured quadrature accuracy was below 3° only between 4 and 5 GHz. The quadrature output at 4.9 GHz is shown in Figure 4.12. The measured phase error at this frequency was about 1.3°. The measurement results show that it's possible to obtain quadrature phases through tail current coupling without any parallel coupling paths. A picture of the measurement set-up in the lab is shown in Figure 4.13, which was used for the phase noise measurement. The phase noise obtained at 4.9 GHz is shown in Figure 4.14. The measured value was around -123.2 dBc/Hz at 1MHz offset frequency. The measured phase noise vs frequency plot is shown in Figure 4.15. The measurement results show that the phase noise throughout the tuning range was below -120 dBc/Hz. Though simulation results predict a decrease in the phase noise with reduction in frequency, the mismatch could be possible because of modeling of inductors. If the Q factor of the inductor was low, then at low frequencies, it's possible to obtain higher phase noise. It was observed in post-layout simulations that the parasitics were higher than expected which reduced the tuning range to 4-5GHz. The

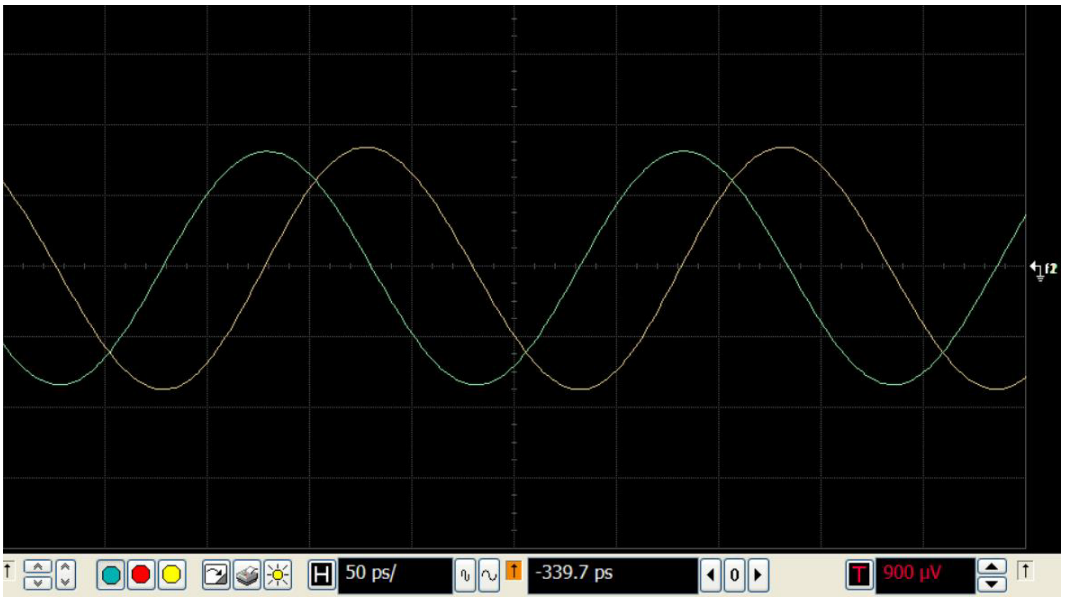

Figure 4.12: Measured Quadrature outputs at 4.9 GHz

measured phase error vs frequency plot is shown in Figure 4.16. A maximum quadrature error of 3 ° was observed across frequencies. The measured phase error vs I_{tail} is shown in Figure 4.17. The measured quadrature error reduces with increase in the tail current, as this increases the swing and reduces the ON duration of the switches, as expected based on simulation results. This reaches a minimum value of 1.4 ° at 4.9 GHz output frequency.

The table of comparison showing the performance of the proposed architecture with other architectures is shown in Table 4.1. The proposed topology offers a competitive FOM of 188.3 dBc/Hz and the core QVCO consumes a power of 7.5 mW from a 1.1 V supply. Better phase noise numbers are expected for the same power consumption if higher metal layers are available. The QVCO is still functional at 0.9 V with without severe phase error degradation though the phase noise is more. The core QVCO consumes a total area of $0.33\ mm^2$.

Table 4.1: Table of Comparison

	Process Range (CMOS)	Tuning GHz	VDD V	Phase Noise dBc/Hz @1MHz	at f_{osc} GHz	FOM dBc/Hz	Power mW
RFIC 2014 [15]	65nm	2.75-6.25	0.6	-128	3	188	9.36
TCASII 2015 [16]	180nm	2.2-2.5	1.8	-128	2.4	192	2.67
MTT 2013 [1]	130nm	4.4-5.4	1	-121	5	189	4.2
JSSC 2013 [6]	180nm	4.74-4.85	1.2	-125	4.84	193	3.4
JSSC 2017 [17]	65nm	7.6-8.3	0.8	-120	7.9	186.6	27.2
ESSCIRC 2015 [18]	65m	7.7-8.7	0.6	-120.9	8.2	188.4	12.3
This work	40nm	4-5	1.1	-123.2	4.9	188.3	7.5

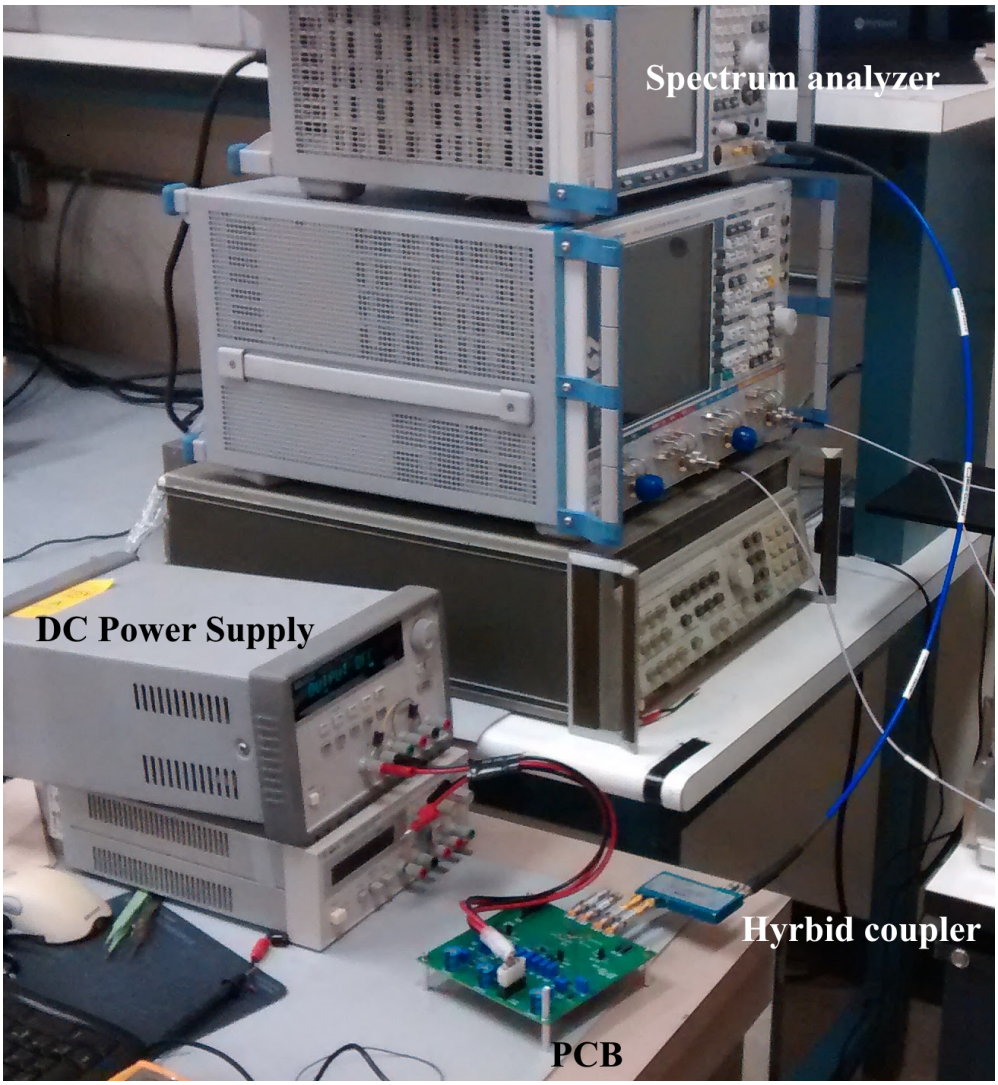

Figure 4.13: Lab measurement set-up for phase noise measurement

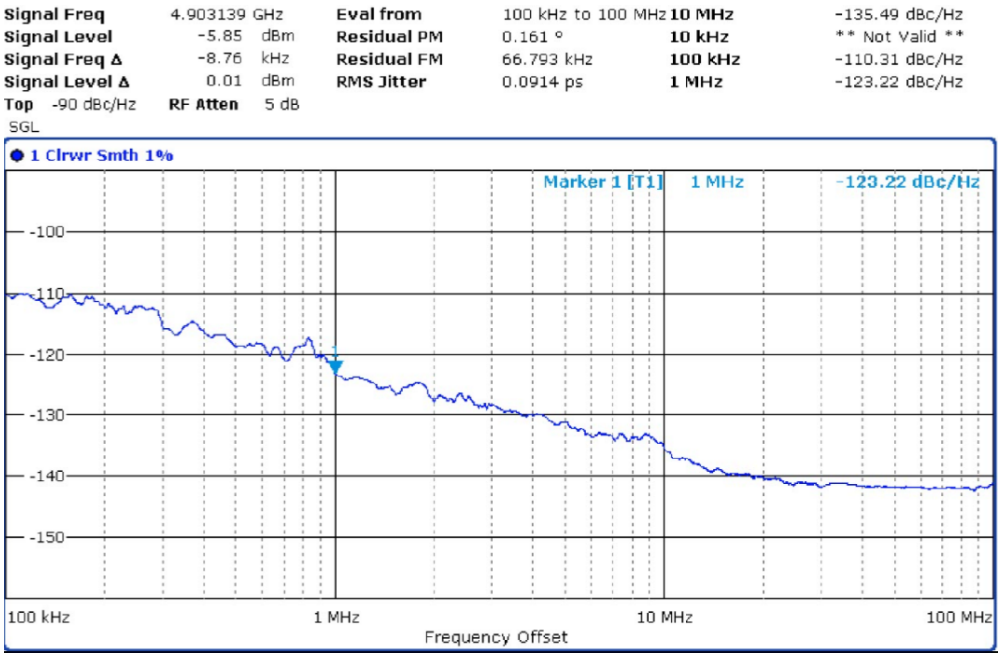

Figure 4.14: Measured phase noise at 4.9GHz frequency

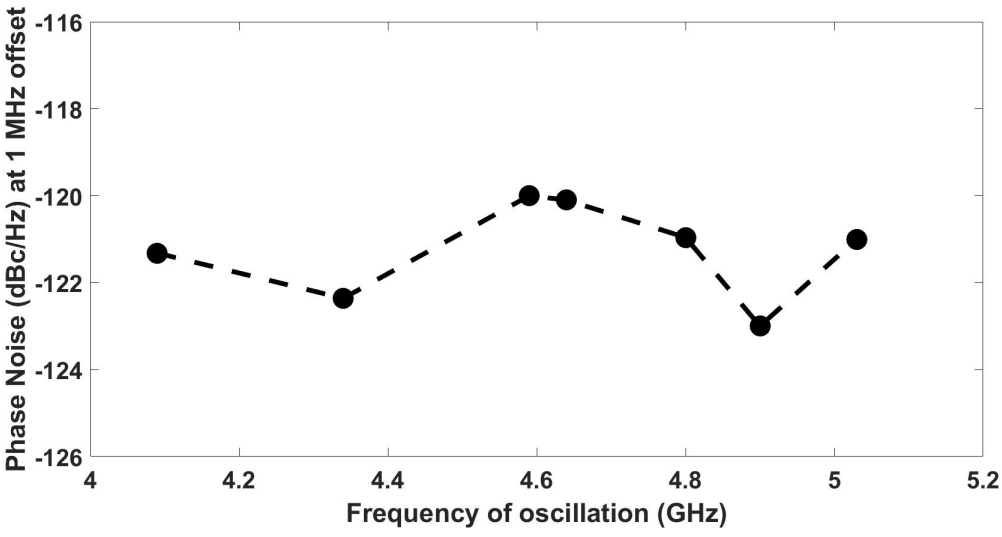

Figure 4.15: Measured phase noise vs frequency

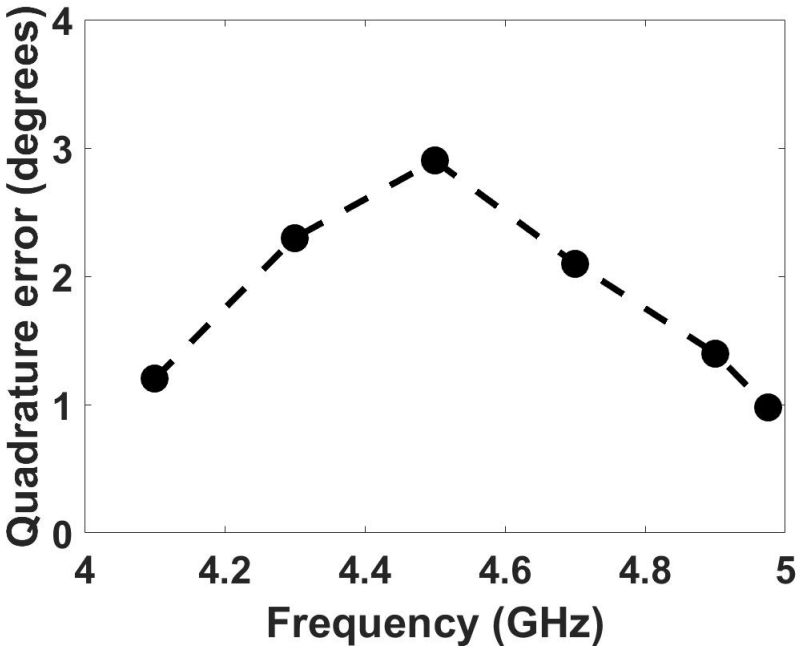

Figure 4.16: Measured Quadrature error vs frequency

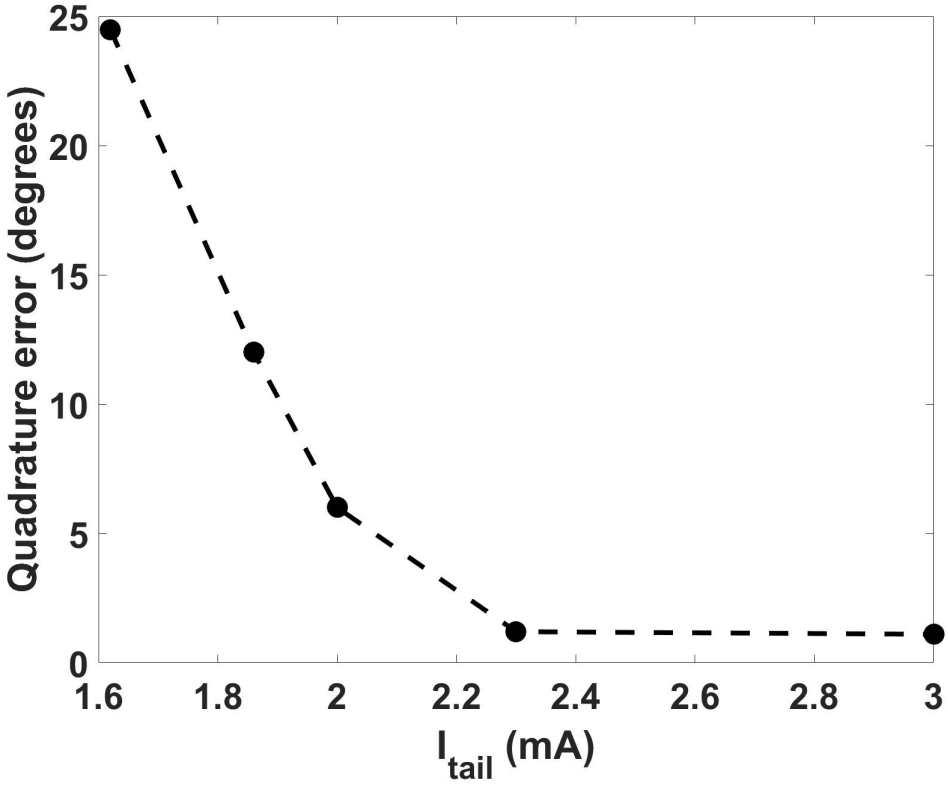

Figure 4.17: Measured Quadrature error vs I_{tail} at 4.9 GHz output frequency

5. CONCLUSION

This thesis proposed a new architecture for QVCO using a novel tail current-clipping technique. The proposed architecture has several highlighted advantages over P-QVCO structure due to the absense of the traditional coupling network. Simulation and measurement results indicate that the proposed structure outperforms the P-QVCO structure in terms of phase noise performance and power consumption. The proposed circuit eliminates off-resonance behavior while ideally is better than a P-QVCO in terms of phase error. Future work can be made on innovative switching coupling techniques and wave shaping that could result in improvement in tail current shaping while obtaining good phase noise and phase accuracy. The possibility of exploiting the proposed idea to other classes of oscillators can also be explored.

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